High-Thermal-Conductivity (1.8 W/(m·K)) Dry-Film Solder Resist at 20 µm Thickness: Compatible with Standard Process Flow and Steady-State Thermal Validation

Takumi Suzuki, Kohei Kitagawa, Ryohei Nojima, Fumitaka Kato and Daichi Okamoto
Taiyo Ink Mfg. Co., Ltd.
388 Ohkura, Ranzan-machi, Hiki-gun, Saitama 255-0222, Japan
Ph: 81-493062-7777; Fax: 81-493-62-2330
Email: suzuki.takumi@taiyo-hd.co.jp, daichi.okamoto@taiyoink.co.jp

Zihao Lin, Kyoung-Sik Moon, Mohanalingam Kathaperumal and Chin-Ping Wong
Georgia Institute of Technology
Atlanta, Georgia, USA
Email: jack.moon@gatech.edu, kmohan@ece.gatech.edu, cp.wong@mse.gatech.edu

Abstract

Thermal management in compact AI/edge modules increasingly relies on heat conduction through the package stack, where solder resist (SR) can become a thermal bottleneck. This work presents a photosensitive dry-film high-thermal-conductivity solder resist (HTCSR) for IC-substrate integration, providing an isotropic thermal conductivity of 1.8 W/(m·K) at a thickness of 20 µm (≈9× that of a conventional package SR, ~0.2 W/(m·K)) while remaining compatible with a standard lamination–exposure–alkaline development–thermal cure process. The HTCSR exhibits a pronounced melt-viscosity decrease to the same order of magnitude as that of a packaging-grade reference SR, enabling reliable lamination and void-free gap filling on fine Cu patterns (L/S = 12/13 µm). It also achieves low cured-surface roughness and 100-µm opening patternability. Insulation reliability was confirmed by b-HAST (130 °C/85%RH/5 V, L/S = 20/15 µm) using Weibull TTF analysis (n = 6), showing comparable characteristic life (η = 452 h vs. 444 h) and MTTF (437 h vs. 439 h) to the reference SR based on a failure criterion of insulation resistance < 1.0×10^6 Ω. In steady-state thermal tests using a heater/cold-plate fixture, replacing only the SR with HTCSR reduced the equilibrium temperature by 8.5 °C at 0.5 W, as supported by IR thermography showing enhanced lateral heat spreading and a reduced thermal gradient across the SR layer. The results demonstrate a practical route to thermally improved, thin substrate build-up without compromising patternability or insulation reliability.

Key words

Advanced packaging, High insulation reliability, High planarity and embeddability, Solder resist, Steady-state thermal validation, Thermal management.

I. Introduction

The increase in AI-enabled perception and edge-computing systems is driving demand for high-density electronic modules in which the adoption of conventional heat sinks (Fig. 1) is limited by form-factor and integration requirements [1], [2]. Under such constraints, heat conduction through the package stack plays an increasingly important role, and thermal dissipation frequently involves dielectric-contact interfaces [3]. Since elevated junction temperatures degrade performance and reliability (e.g., increased leakage current, higher noise, and reduced timing margins), lowering the thermal resistance within the package is a key requirement. Nevertheless, conventional solder resists (SRs) are typically engineered for electrical insulation, chemical robustness, and fine patterning, rather than for package-level thermal management [4]. While die-backside heat extraction has been

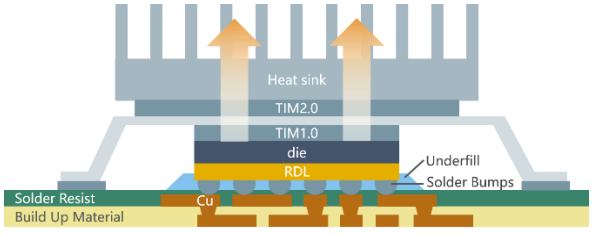


Fig. 1 Schematic drawing of a conventional solution for heat generation from an IC chip.



Fig. 2 Schematic drawing of thermal spreading through High-thermal-conductivity SR layer.

widely explored, systematic studies focusing on substrate-side thermal-management materials remain limited [5-8]. In architectures where the die front side cannot host a heat sink—for example, optics-constrained image modules such as CIS—the substrate becomes the primary heat-extraction path, highlighting the importance of substrate materials.

Previously, chip-temperature reduction has been reported by inserting a thermal spreading layer between the build-up dielectric and the SR (e.g., a 25 µm graphite sheet with a 20 µm adhesive layer), but this requires additional lamination/laser processes and increases total thickness and the risk of electrical short circuits [9]. On the other hand, research on the thermal conductivity of solder resist has been limited to PCB applications [10], and reports on thermally conductive solder resist specifically developed for package-substrate applications remain very limited.

To address these gaps, we develop and evaluate a high–thermal-conductivity photosensitive dry-film SR (HTCSR) formulated for IC-substrate fabrication (Fig. 2). Compared with our previously reported HTCSR [11], the present work further optimizes the formulation to simultaneously increase thermal conductivity while maintaining a low melt viscosity, thereby enabling reliable gap filling for finer Cu line/space (L/S) patterns; in this study, gap filling was confirmed down to L/S = 12/13 µm. Target specifications include a thermal conductivity, $k \geq 1.8$ W/(m·K) at a thickness of 20 µm (approximately nine times that of conventional package-use SRs with $k \approx 0.2$ W/(m·K)), compatibility with conventional lamination–exposure–alkaline development–thermal cure processing, 100-µm aperture patternability, and surface smoothness suitable for package-substrate applications.

We systematically characterize melt viscosity vs. temperature for process compatibility, embeddability and gap filling over an L/S = 12/13 µm Cu pattern, surface planarity/roughness, and insulation reliability via a biased highly accelerated temperature and humidity stress test (b-HAST) using time-to-failure measurements and Weibull statistics (130 °C/85%RH/5 V, L/S = 20/15 µm). We then quantify steady-state thermal performance using a controlled heater/heat-sink fixture with IR thermography and temperature sensing, isolating the impact of SR replacement only on equilibrium temperature under fixed power dissipation. This study demonstrates that substrate-side thermal mitigation is achievable without altering baseline substrate fabrication flows and provides clear, quantitative evidence of temperature reduction attributable to the SR layer itself.

II. Experimental Section

A. Process Compatibility Assessments as a Solder Resist

First, the process compatibility was evaluated through melt-viscosity measurements, development testing, and embeddability assessments on the substrates.

The test sample for measuring the melt viscosity of the HTCSR was prepared by repeated lamination of the dry film using a roll laminator (TAISEI LAMINATOR, VA-770) until a total thickness of 200 µm was obtained. Then, their melt viscosity values were measured using a rheometer (Thermo Scientific HAAKE, RheoStress 6000).

In order to confirm the resolution performance of the HTCSRs, dry film HTCSRs of 20 µm thickness were vacuum laminated onto copper clad laminate (CCL). After the lamination, the HTCSRs were exposed to 50 – 250 mJ/cm^2 of UV light (365 nm) with an exposure machine (ORC, Mms504D). Then, the HTCSRs were developed with 1.0 wt% Na_2CO_3aq. Subsequently, the HTCSRs were exposed to 1000 mJ/cm^2 as a post UV process and then heated at 160 °C for 60 min for heat curing. The vias were observed using a scanning electron microscope (SEM).

The gap-filling capability and embeddability were evaluated by vacuum lamination of HTCSRs onto a substrate with a pattern of L/S = 12/13 µm. After that, HTCSRs were exposed to 1000 mJ/cm^2 as a post-UV process and then heated at 160 °C for 60 min for thermal curing. The cross section of the substrate with the HTCSR laminated on the pattern was observed using SEM.

B. Thermal Characterization

The thermal conductivity values listed below were calculated from (1) using the measured values of the specific heat capacity, density, and thermal diffusivity.

$$K = \rho \cdot C_p \cdot \alpha \qquad (1)$$

Here, K is the thermal conductivity of the material (W/(m・K)), ρ is the mass density (kg/m^3), C_p is the specific heat capacity at constant pressure (J/(kg・K)) and α is the thermal diffusivity (m^2/s).

For measurement of the specific heat capacity, density, and thermal diffusivity, a 20-µm-thick dry-film HTCSR was repeatedly laminated onto a copper foil and exposed to UV light at 400 mJ/cm² (365 nm) using a maskless aligner (ORC, Mms504D). This lamination-exposure sequence was repeated five times. After the final lamination step, the stack was additionally exposed to UV light at 1000 mJ/cm^2 (365 nm) and then thermally cured at 160 °C for 60 min. Finally, the sample for measurement was obtained by peeling off from the copper foil. The specific heat capacity was measured using DSC (TA Instruments, DSC Q100). The density was determined using an electronic densimeter (Alfa Mirage, SD-200L). The thermal diffusivity was measured using a periodic-heating thermal diffusivity measurement system (ADVANCE RIKO, FTC-RT).

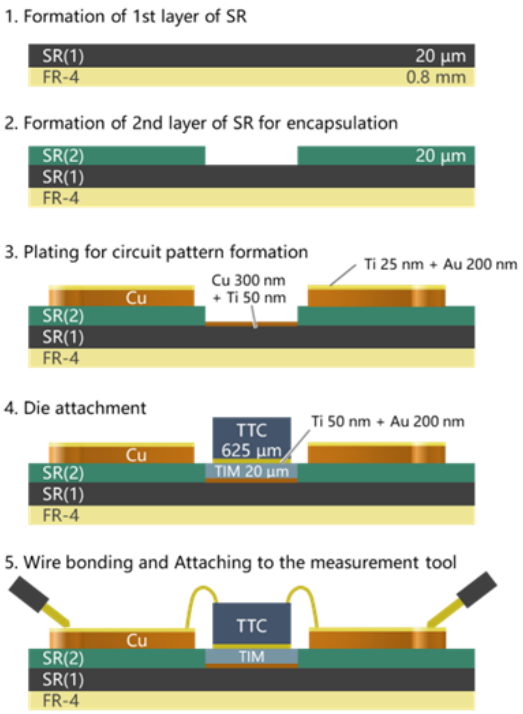


Fig. 3 Schematic side view of the processes used to fabricate the test vehicle for evaluation of thermal spreading of SR. The thickness of FR-4, SR(1), SR(2), Cu pattern, TIM and TTC are 0.8 mm, 20 µm, 20 µm, 7 µm, 50 µm and 625 µm, respectively.

To evaluate the thermal dissipation in the TTC and SR layers, the test vehicle was fabricated on 2-inch FR-4 substrate by formation of SR, plating Cu pattern, die attachment and wire bonding (Fig. 3 and 4(a)).

A 20-µm-thick HTCSR dry film was laminated onto an FR-4 substrate (0.8 mm thick), exposed to UV light at 100–250 mJ/cm² (375 nm) using a maskless aligner (Heidelberg Instrument, MLA150), and thermally cured at 160 °C for 60 min. The HTCSR layer was subsequently exposed to 1000 mJ/cm² UV light (375 nm) as a post-UV process to form the first solder resist layer (SR(1)). Next, a commercially available 20-µm-thick dry-film solder resist, used as the reference material in this study, was vacuum-laminated onto SR(1) and UV-exposed prior to development to form the second solder resist layer (SR(2)). An opening was patterned at the center of SR2 to define the attachment area for the thermal test chip (TTC). This configuration enables evaluation of heat dissipation from the TTC through SR(1). In addition, SR2 (thermal conductivity: 0.2 W/(m·K)) served as an encapsulation layer to suppress heat loss from SR(1) to ambient air and to the substrate copper wiring.

Prior to TTC attachment, a Ti/Cu seed layer was deposited on SR(2) by sputtering, followed by Cu electroplating to form the routing patterns. To further improve wire-bondability and interfacial adhesion, a Ti/Au metallization layer was deposited by e-beam evaporation (Ti: 25 nm; Au: 200 nm) on the bonding areas. For die attach, a thermal interface material (TIM) layer of 20-µm thickness (UNIMEC XH9888-1) was uniformly applied onto the die-attach area to promote a controlled and repeatable thermal contact. Subsequently, the TTC was attached onto SR(1) using an Ag sinter paste process.

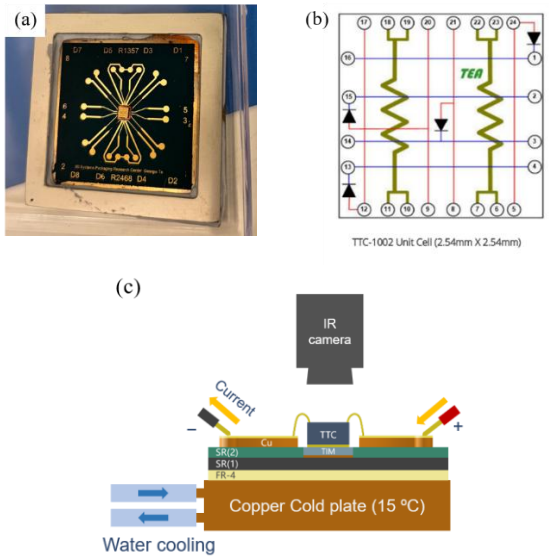


Fig. 4 (a) Fabricated thermal test vehicle with the TTC, (b) schematic drawing of unit cell of TTC-1002 and (c) schematic drawing of a controlled heater/heat-sink fixture with IR camera.

The TEA thermal test chip (TTC-1002) used in this study is shown in Fig. 4(b). The TTC-1002 has a die size of 2.54 mm × 2.54 mm and a die thickness of 625 µm. It integrates two resistive heaters, each capable of dissipating up to 6 W (12 W total maximum), and includes four thermocouple diodes for temperature sensing [12]. Finally, electrical interconnection was completed by Au wire bonding.

The vehicle was characterized under controlled steady-state power loads of up to 0.6 W. After fabrication, the test vehicle was mounted on a water-circulated copper cooling plate, and current was supplied to the on-chip resistor to generate Joule heating. Under steady-state conditions, surface temperature fields (including the TTC region) were measured using infrared (IR) thermography (Fig. 4(c)).

C. Insulation Reliability Assessment of Solder Resist

To evaluate insulation reliability, a b-HAST was performed using substrates coated with SR. A substrate with fine-pitch comb-shaped wiring patterns (L/S = 20/15 µm) was used (Fig. 5). The test conditions were as follows: SR thickness, 20 µm; temperature, 130 °C; relative humidity, 85%RH; test duration, 200 h; bias voltage, 5 V DC. Four samples were tested for each SR. Failure was defined as an insulation resistance below 1.0×10^6 Ω.

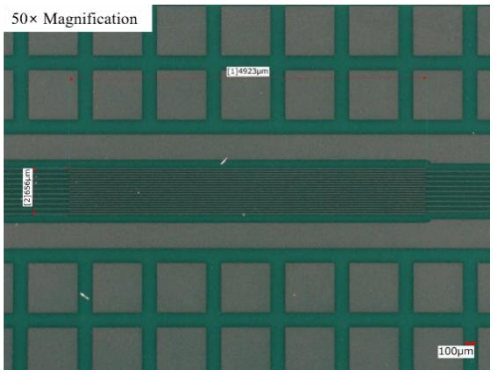


Fig. 5 The substrate for reliability test with the copper pattern (L/S = 20/15 µm).

III. Results and Discussion

A. Process Compatibility Assessments as a Solder Resist

First, the melt viscosities of dry-film SRs with different filler loadings were measured using a rheometer. By formulation optimization aimed at simultaneously retaining high thermal conductivity and rheology tuning for vacuum lamination, the HTCSR (k = 1.8 W/(m·K)) exhibited a marked reduction in melt viscosity around 100 °C—an appropriate temperature range for lamination—reaching the same order of magnitude as the packaging-grade reference SR (Fig. 6).

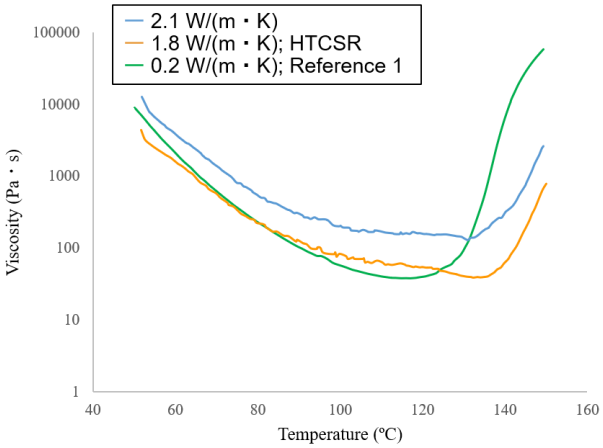


Fig. 6 Melt viscosity of dry film samples along with their thermal conductivity and relative filler content. The reference is a sample used for packaging-grade applications.

Next, the embeddability of 1.8 W/(m·K) dry-film HTCSR was confirmed by vacuum lamination onto a substrate with copper patterns (L/S = 12/13 µm) at 110 °C (Fig. 7). This result extends our previous report [11], in which void-free filling was evaluated using an HTCSR with k = 1.2 W/(m·K) and the finest Cu pattern tested was L/S = 20/20 µm. The cross-sectional image showed that the SR surface exhibited negligible surface topography or voids at the copper edges, and the Cu trenches were completely filled with HTCSR without observable void formation.

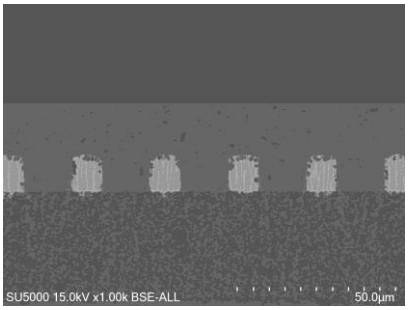


Fig. 7 Cross sectional SEM image of the substrate after lamination of HTCSR (1.8 W/(m·K)) of 20 µm dry film thickness on the copper pattern (L/S = 12/13 µm).

For the HTCSR of 1.8 W/(m·K), a target opening diameter of 100 µm was achieved (Fig. 8). The opening diameters were 105 and 98 µm at the top and bottom, respectively. No residual HTCSR was observed on the CCL surface after development.

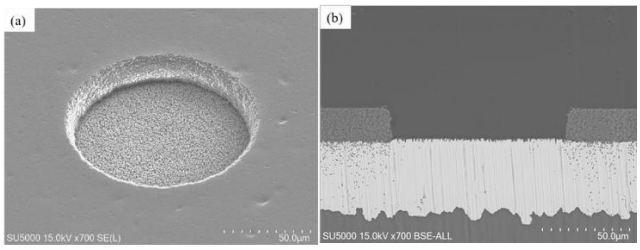


Fig. 8 (a) Top view and (b) cross-sectional SEM images of HTCSR after an exposure of 180 mJ/cm^2 and development in 1.0wt% Na_2CO_3aq.

Fig. 9 compares the cured-surface roughness Sa measured by a 3D profilometer (Keyence VK-X3000). The present HTCSR achieves Sa = 0.14 μm, which is lower than reference 1 (package SR; Sa = 0.19 μm) and much lower than reference 2 (liquid-type thermally conductive SR; Sa = 0.79 μm). While Sa is slightly higher than that of our previous HTCSR (Sa = 0.11 μm) [11], the surface remains comparable to general-purpose package SRs. The particle-size/thermal-conductivity trade-off and the mitigation concept are discussed in detail in [11].

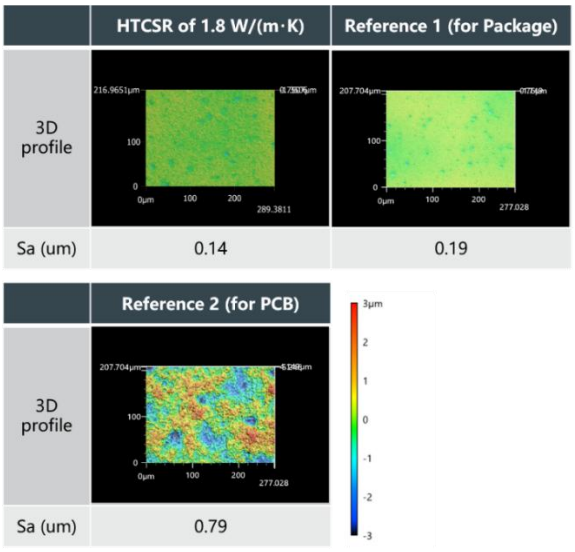


Fig. 9 3D profile images and Sa values of HTCSR of 1.8 W/(m·K), reference 1(dry film SR for package substrate) and reference 2 (liquid SR for PCB substrate of 2.0 W/(m·K)). The SR thickness of each sample was 20 μm.

B. *Thermal Characterization*

The HTCSR enables more efficient heat dissipation than the reference package SR, resulting in a lower equilibrium temperature and reduced thermal resistance under higher-power operation. At an input power of 0.5 W (corresponding to an operating power density of 7.75 W/cm²), the equilibrium temperature decreased from 96.0 °C (reference SR) to 87.5 °C with the HTCSR (k = 1.8 W/(m·K)), i.e., an 8.5 °C reduction (Fig. 10), The reported values were obtained from one representative test vehicle for each material condition. Additional repeat testing is planned for future work.

Consistently, the extracted thermal resistance was reduced from 152 °C/W to 139 °C/W compared with the reference. These results confirm the superior heat-dissipation capability of the HTCSR composite under high-power operation.

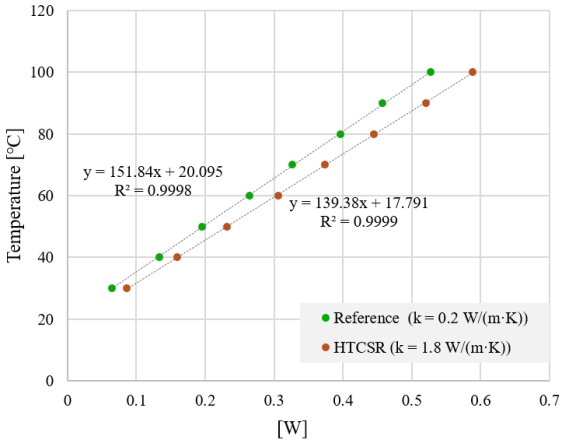


Fig. 10 Results of steady-state tests for the thermal performance of the HTCSR with the TTC. The thermal conductivity of HTCSR and reference sample are 1.8 and 0.2 W/(m·K), respectively.

To further assess heat dissipation under transient conditions, Fig. 11 compares the chip cool-down behavior after switching off the heater while the substrate was placed on a 15 °C Cu cold plate. Both samples start at 100 °C at 0 s; however, the HTCSR cools more rapidly, reaching 38.0 °C at t = 5 s, whereas the reference SR remains at 46.9 °C. This corresponds to an 8.9 °C lower chip temperature for the HTCSR at 5 s, indicating enhanced heat transfer from the chip through the substrate stack during cooling. Together with the steady-state temperature reduction and lower extracted thermal resistance in Fig. 10, these transient results further substantiate the superior heat-dissipation capability of the HTCSR composite.

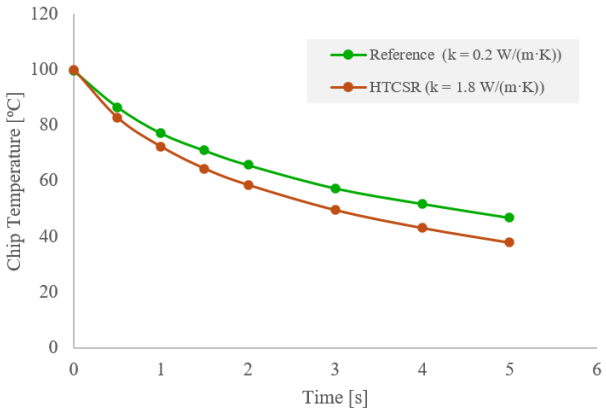


Fig. 11 Transient chip temperature during post-heating cooling after the heater was switched off at 0 s for the reference package SR and the HTCSR sample. The substrate was placed on a Cu cold plate maintained at 15 °C, and the chip temperature was monitored over 0–5 s from an initial temperature of 100 °C.

C. Insulation Reliability

To evaluate insulation reliability, b-HAST testing was conducted, and the time-to-failure (TTF) data were analyzed using Weibull statistics (Fig. 12). Failure was defined as the insulation resistance dropping below 1.0×10^6 Ω. For the HTCSR sample (k = 1.8 W/(m·K)), the Weibull parameters were m (shape) = 16.0 and η (characteristic life) = 452 h, whereas the reference exhibited m = 51 and η = 444 h (n = 6 each). Despite differences in the fitted shape parameter, both materials exhibited comparable characteristic life and MTTF values (437 h for HTCSR and 439 h for the reference). The proximity of the Weibull distributions suggests that replacing only the SR with HTCSR does not degrade insulation lifetime within the evaluated design rule (L/S = 20/15 µm) and test bias (5 V).

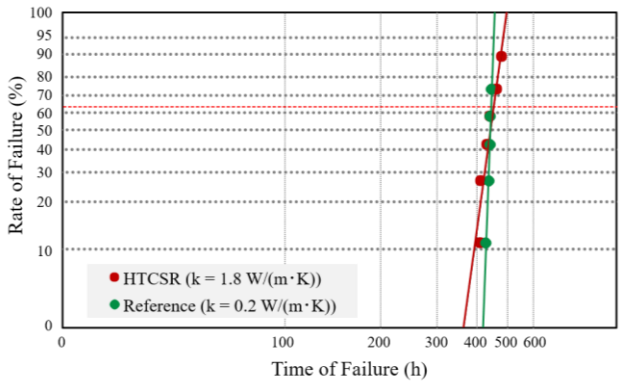


Fig. 12 Weibull plot of insulation time-to-failure (TTF) obtained from b-HAST testing for HTCSR (brown, n = 6, k = 1.8 W/(m·K)) and the reference (green, n = 6) using the L/S = 20/15 µm pattern. Test conditions: 130 °C, 85%RH, 5 V. Failure was defined as an insulation resistance < 1.0×10^6 Ω. Lines indicate Weibull fits.

IV. Conclusion

We introduced a photosensitive dry-film high-thermal-conductivity solder resist (HTCSR) designed for IC-substrate integration. Building on our previously reported HTCSR, the present work optimized the formulation to achieve higher thermal conductivity while maintaining a low melt viscosity, thereby improving lamination processability and enabled void-free gap filling on finer Cu patterns; in this study, gap filling was confirmed down to L/S = 12/13 µm. The material achieved an isotropic thermal conductivity of 1.8 W/(m·K) at a thickness of 20 µm while maintaining manufacturability within a standard lamination–exposure–alkaline development–thermal cure flow, low cured-surface roughness, and 100-µm opening patternability. Insulation reliability was evaluated by b-HAST (130 °C/85%RH/5 V) using Weibull analysis of time-to-failure (TTF), where failure was defined as insulation resistance < 1.0×10^6 Ω (L/S = 20/15 µm; n = 6 each). The fitted characteristic lives were comparable (η = 452 h for HTCSR vs. 444 h for the reference), consistent with nearly identical MTTF values (437 h vs. 439 h), indicating no observable degradation in insulation lifetime due to replacing only the SR with HTCSR. Steady-state thermal benchmarking using a controlled test vehicle confirmed that replacing only the SR with HTCSR reduced the equilibrium temperature by 8.5 °C at 0.5 W compared with a general SR, and IR thermography indicated enhanced lateral heat spreading and a reduced through-plane thermal gradient across the SR layer. Although the SR thermal conductivity increased by ~9× (from ~0.2 to 1.8 W/(m·K)), the reduction in the extracted overall thermal resistance was more modest (152 to 139 °C/W) because the SR layer constitutes only one segment of the total heat-flow path; other contributions include the heater/TIM contact, substrate dielectrics and Cu routing, and interfacial thermal resistances. In addition, the present measurements do not quantitatively separate through-plane and lateral contributions, and statistical significance across multiple vehicles will be addressed through repeat testing and thermo-mechanical/thermal simulations in future work. Collectively, these results establish HTCSR as a practical, process-compatible route to substrate-side thermal management in compact modules, enabling meaningful temperature reduction without added stack-up layers or process complexity. Future work will extend transient characterization to power-cycling and dynamic workloads, and will further investigate finer-feature patterning limits. In addition, we will investigate deployment in high-power edge/AI assemblies where thermally conductive SRs can improve system-level thermal margins.

Acknowledgment

This work was supported by the Georgia Institute of Technology 3D Systems Packaging Research Center (GT-PRC). The authors gratefully acknowledge the GT-PRC members and consortium for their cooperation and support, in particular Prof. Y. Joshi, Prof. G. Yushin, Dr. W. Fu, M. Bouzidi, C. Hu, and H. Park for their vital support with test-vehicle fabrication and thermal experiments. Additionally, the authors thank Dr. D. Shangguan of Thermal Engineering Associates (TEA) for valuable technical discussions.

References

[1] T. Zhou, S. Ma, D. Yu, M. Li and T. Hang, "Development of Reliable, High Performance WLCSP for BSI CMOS Image Sensor for Automotive Application", Sensors, 2020, 20(15), 4077.

[2] H. Hsiao, "Role of Adhesive Modulus on Reliability of FCBGA with Heat Spreader", 2002 Int'l Symposium on Electronic Materials and Packaging, 2002, pp. 161-166.

[3] V. Kodukula, S. Katrawala, B. Jones, C. Wu and R. LiKamWa, "Dynamic Temperature Management of Near-Sensor Processing for Energy-Efficient High-Fidelity Imaging", Sensors 2021, 21(3), 926.

[4] C. Ueta, K. Okada, T. Shiina, T. Hanada and N. Ito, "Development of Solder Resist with Improved Adhesion at HTSL (175 deg C for 3000 Hours) and Crack Resistance at TST for Automotive IC Package", 2017 IEEE 67th Electronic Components and Technology Conference (ECTC), 2017, pp. 156-165.

[5] M. Sasaki, R. Kikuchi, T. Sakai and S. Sakuyama, "Evaluation of Thermal Resistance for Underfill Layer in Three-dimensional Stacked ICs by Transient Thermal Analysis", Smart Process, Vol. 7, 2018.

[6] Y. Wen, C. Chen, Y. Ye, Z. Xue, H. Liu and Y. Mai et al., "Advances on Thermally Conductive Epoxy-Based Composites as Electronic Packaging Underfill Materials—A Review", Adv. Mater. 2022, 34, 2201023.

[7] A. Zinn, N. Ngo, H. Zinn, K. Nguyen, R. Stoltenberg et al., "Large, High Conductivity Direct-Fill Copper Thermal Vias for High Power Devices", 2022 IEEE 72nd Electronic Components and Technology Conference (ECTC), 2022, pp. 1238-1243.

[8] Y. Fang, T. Liu and D. Sun, "Research on Novel Thermal Management Technology in the Field of Integrated Circuits", 2024 25th International Conference on Electronic Packaging Technology (ICEPT), 2024, pp. 1-6.

[9] K. Matsumoto, D. Oshima, H. Mori, A. Watanabe, R. Budd, D. Edelstein, et al., "Graphite Sheet Embedded in an Organic Flip-Chip Package for Heat Spreading", 2025 IEEE 75th Electronic Components and Technology Conference (ECTC), 2025, pp. 467-472.

[10] S. Cho, J. Y. Lee, "Heat Dissipation of Printed Circuit Board by the High Thermal Conductivity of Photo-Imageable Solder Resist", Electronic Materials Letters, Vol. 6, 2010, pp. 167-172.

[11] T. Suzuki, K. Kitagawa, D. Okamoto, Z. Lin, K. Moon, C. Wong, et al., "High-Thermal-Conductivity (1.0 W/(m·K)) Dry-Film Solder Resist at 20 μm: Compatible with Standard Process Flow and Steady-State Thermal Validation", 2026 IEEE 76th Electronic Components and Technology Conference (ECTC), 2026, pp. 700-705.

[12] C. Fu, K. Moon, A. Ketterson, and M. Tentzeris, "Thermal Characterization and Benchmarking of Aluminum Ribbon Ceramic (ARC) Substrates in mmWave/RF Packaging Applications", 2025 IEEE 75th Electronic Components and Technology Conference (ECTC), 2025, pp. 2307-2312.