THERMAL TEST CHIPS

TTC-1002A

(2.5mm X 2.5mm Unit Cell)
Wire Bond or Flip Chip

DESCRIPTION

The TTC-1002 thermal test chip is designed to provide a maximum of flexibility for thermal characterization of semiconductor packages. Each Unit Cell can be used individually or in a square or rectangular array. Strategically placed diode temperature sensors enable temperature measurements to be made in the center, corner and mid-side of an individual die or any configuration array. All diodes, whether in a single die or arrayed die configuration, can be individually addressed, allowing for temperature contour measurements across a Unit Cell or an array. The two heating resistors on each die can be powered individually or wired in a series or parallel configuration for operation from a single power supply. In an array configuration, there are several resistor series strings that can be individually powered from separate power supplies or paralleled for operation from a single supply. The multiple resistor design allows for thermal measurements with non-uniform heating across the die or array.

FEATURES

- **Proven silicon technology**
- **Format: bumped/flip chip or wire bond wafers or arrays of Unit Cells**
- **Kelvin connections to heating resistors for improved measurement accuracy**
- **Array form factor: may be arrayed square or rectangular**
- **Wire bond: on-chip adjacent cell interconnections of resistors and sensors providing for parallel or series or parallel/series resistor connections with peripheral pad wire bonding**
- **Bumped: all resistors and sensors may be individually connected**
- **Two resistors and four sensors per Unit Cell; many resistors and sensors in arrays**
- **Uniform and non-uniform heating and planar temperature contours capable**
- **Suitable for both steady-state and transient thermal measurements**

Contact TEA for:

- ► **Re-Distribution Layer (RDL) options**
- ► **Bump material composition options, including copper pillars**
- ► **Backside metal and thinning/polishing options**

SPECIFICATIONS

Electrical - Heating	TTC-1002
# of Resistors	2
Resistance Value	7.6 Ω ±10 % (each resistor)
Resistance Variation	±10% (for die from a specific wafer)
Heating Resistor Power Dissipation (each resistor) for $T_J \leq 150°C$	12.8W (~9.9V @ ~1.30A) max for 1ms 10.9W (~9.1V @ ~1.2A) max continuous
Power Density (per Cell) for $T_J \leq 150°C$	398W/cm^2 max for 1ms 338W/cm^2 max continuous
Connection	Force & Sense wire bond or bump pads
Resistor Coverage	>85% of die area within wire bond pads

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SPECIFICATIONS (continued)

Electrical - Sensing	TTC-1002
# of Diodes	4 (1 center, 2 opposing corners, 1 mid-side)
Nominal V_F	0.71V @ I_F = 1mA each diode
Nominal BV_R	5V @ I_R = 10µA each diode
Addressing	Row and Column wire bond or bump pads
Physical	
Wafer Size	200 mm (8 inch) Diameter Nominal
Unit Cell Size	2.54 x 2.54 mm (0.10 X 0.10 inch)
Die Layout	See Figure 1
Array Capability	See Figure 3
Wafer Thickness	725µm (0.029 inch) Nominal **(thinning optional)**
Scribe Line Width Between Cells	76µm
Wafer Backside Finish	Ground, un-polished **(polishing optional)**
Wafer Yield	Greater than 80% (Center 127X127mm (5"x5") square area only)
Approximate Unit Cells/Wafer	>2500 in center area
Wire Bond Pad Size	150µm (0.00654 inch) diameter
Wire Bond Pad Material	Al-Si(1.0%)-Cu(0.5%)
Bump Material (other types optionally available)	Lead-free solder bump, or Cu pillar with solder cap
Bump Size (other sizes optionally available)	Solder bump: ~105µm diameter, ~80µm height Cu pillar: ~90µm diameter, ~50µm height + ~20µm solder cap

Figure 1 Unit Cell Layout

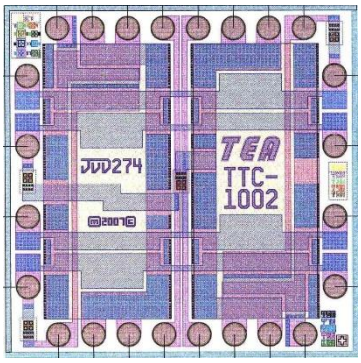


Figure 2 Unit Cell Schematic Representation

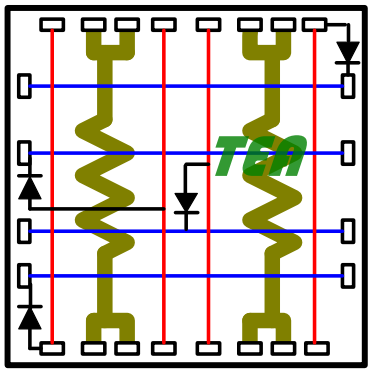
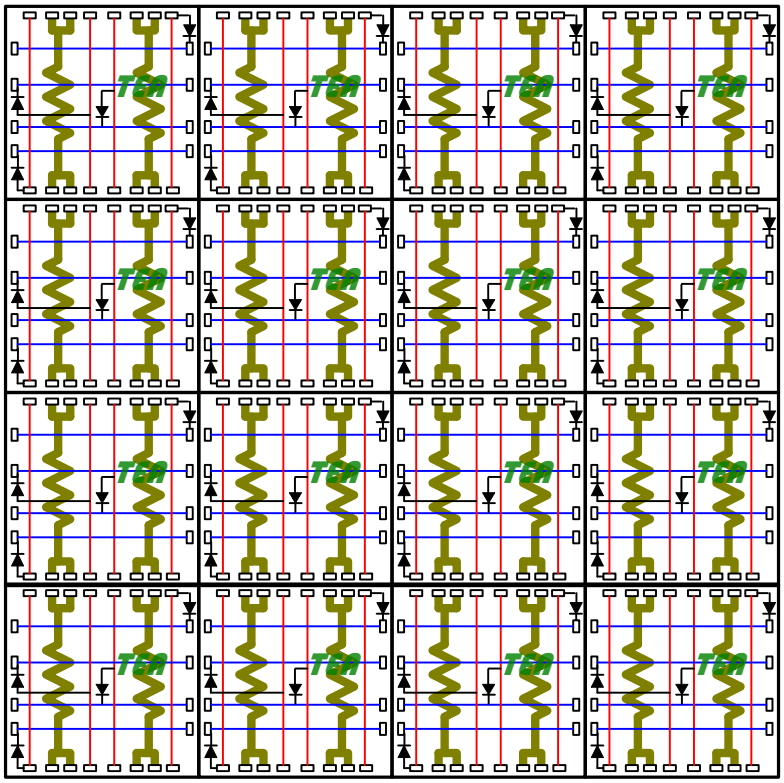


Figure 3 Typical Array Layout (Shown as 4 X 4 array)



For assistance in electrical connection of Unit Cells in an array configuration, please contact TEA with your specific array requirements.