METHOD 3101.3

THERMAL IMPEDANCE (RESPONSE) TESTING OF DIODES

1. Purpose. The purpose of this test is to determine the thermal performance of diode devices. This can be done in two ways, steady-state thermal impedance or thermal transient testing. Steady state thermal impedance (referred to as thermal resistance) determines the overall thermal performance of devices. A production-oriented screening process, referred to as thermal transient testing, is a subset of thermal impedance testing and determines the ability of the diode chip-to-header interface to transfer heat from the chip to the header, and is a measure of the thermal quality of the die attachment. It is relevant to designs which use headers, or heat conducting plugs, with mass and thermal conductivity allowing effective discrimination of poor die attachments. This is particularly true with power devices. The method can be applied to rectifier diodes, transient voltage suppressors, power zener diodes, and some zener, signal and switching diodes. This method is intended for production monitoring, incoming inspection, and pre-burn in screening applications. Some zener constructions, particularly when used with small junction area designs, cool too rapidly (from a heating current) to provide accurate measurement when forward (diode) current is used for this test. For such devices, a method is provided to apply currents in the zener direction and make a measurement much closer to the termination of the heating current. In this way, no minority carriers are involved and inductive effects are minimized due to lower test current. This may be considered a lab measurement because cable lengths in an ATE may prevent accurate measurements so close to cessation of the heating current. This laboratory method is intended on initial zener device design verification for correlation to forward direction thermal impedance testing (such as with ATE) prior to establishing a production test limit. Correlation assurance must be provided in the forward production monitoring that thermal impedance in the reverse direction (zener) must not exceed the specified limit. If this zener test method exceeds the forward method by 10 percent or more, production monitoring (with an ATE in the forward direction) will require a lower limit, for some devices, than that required by the more accurate lab method (see 5.1).

1.1 Background and scope for thermal transient testing. Steady-state thermal response (transient thermal impedance) of semiconductor devices are sensitive to the presence of these voids in the die attachment material between the semiconductor chip and package since voids impede the flow of heat from the chip to the substrate (package). Due to the difference in the thermal time constants of the chip and package, the measurement of transient thermal response can be made more sensitive to the presence of voids than can the measurement of steady-state thermal response. This is because the chip thermal time constant is generally several orders of magnitude shorter than that of the package. Thus, the heating power pulse width can be selected so that only the chip and the chip-to-substrate interface are heated during the pulse by using a pulse width somewhat greater than the chip thermal time constant but less than that of the substrate. Heating power pulse widths ranging from 1 to 400 ms for various package designs have been found to satisfy this criterion. This enables the detection of voids to be greatly enhanced, with the added advantage of not having to heat sink the DUT. Thus, the transient thermal impedance or thermal response techniques are less time-consuming than the measurement of thermal resistance for use as a manufacturing screen, process control, or incoming inspection measure for die attachment integrity evaluation.

2. Definitions. The following symbols and terminology shall apply for the purpose of this test method in the forward direction: (When using the zener method, see NOTES below):

a. V_F: The forward biased junction voltage of the DUT used for junction temperature sensing.
NOTE: When using the zener method, delete “forward” and use “zener” bias.
V_{Fi}: The initial V_F value before application of heating power.
V_{Ff}: The final V_F value after application of heating power.

b. ΔV_F The change in the TSP, V_F, due to the application of heating power to the DUT.

c. I_H: The current applied to the DUT during the heating time in order to cause power dissipation.

d. V_H: The heating voltage resulting from the application of I_H to the DUT.

e. P_H: The heating power pulse magnitude; product of V_H and I_H.

f. t_H: The duration of P_H applied to the DUT.

g. I_M: The measurement current used to forward bias the temperature sensing diode junction for measurement of V_F.

NOTE: When using the zener, delete “forward” and use “zener” bias.

h. t_{MD}: Measurement delay time is defined as the time from the start of heating power (P_H) removal to the start of the final V_F measurement time, referred to as t_{SW}.

i. t_{SW}: Sample window time during which final V_F measurement is made. The value of t_{SW} should be small; it can approach zero if an oscilloscope is used for manual measurements.

j. VTC: Voltage-temperature coefficient of V_F with respect to T_J at a fixed value of I_M; in mV/°C.

k. K: Thermal calibration factor equal to the reciprocal of VTC; in °C/mV.

l. CU: The comparison unit, consisting of ΔV_F divided by V_H, that is used to normalize the transient thermal response for variations in power dissipation; in units of mV/V.

m. T_J: The DUT junction temperature.

n. ΔT_J: The change in T_J caused by the application of P_H for a time equal to t_H.

o. $Z_{\theta JX}$: Thermal impedance from device junction to a time defined reference point; in units of °C/W.

p. $Z_{\theta JC}$: Thermal impedance from device junction to a point on the outside surface of the case immediately adjacent to the device chip measured using time equal time constant of device; in units of °C/W.

q. $R_{\theta JX}$: Thermal resistance from device junction to a defined reference point; in units of °C/W.

$R_{\theta JC}$: Thermal resistance from device junction to a point on the outside surface of the case immediately adjacent to the device chip; in units of °C/W.

$R_{\theta JA}$: Thermal resistance from device junction to an ambient (world); in units of °C/W.

*r. TSP: The temperature sensitive parameter of V_F or V_Z.

*s. V_Z: The zener voltage. (Also see note 1.)

NOTES: 1. When using the zener method, the following changes shall further apply to the definitions whenever they appear in the text.

Letter symbols: I_F becomes I_Z
V_F becomes V_{ZL}
V_H becomes V_{ZH}
V_{Fi} becomes V_{ZLi}
V_{Ff} becomes V_{ZLf}
ΔV_F becomes ΔV_{ZL}
wording: “forward” bias becomes “reverse” bias

2. ΔV_F, K, and CU parameter values will be substantially different when using the zener method (as

compared to the forward biased method). Some difference will be observed between zeners with different nominal voltages.

3. Apparatus. The apparatus required for this test shall include the following, configured as shown on figure 3101-1, as applicable to the specified test procedure:

a. A constant current source capable of adjustment to the desired value of I_H and able to supply the V_H value required by the DUT. The current source should be able to maintain the desired current to within ±2 percent during the entire length of heating time.

b. A constant current source to supply I_M with sufficient voltage compliance to turn the TSP junction fully on.

c. An electronic switch capable of switching between the heating period conditions and measurement conditions in a time frame short enough to avoid DUT cooling during the transition; this typically requires switching in the microsecond or tens of microseconds range.

d. A voltage measurement circuit capable of accurately making the V_{Ff} measurement within the time frame with millivolt resolution.

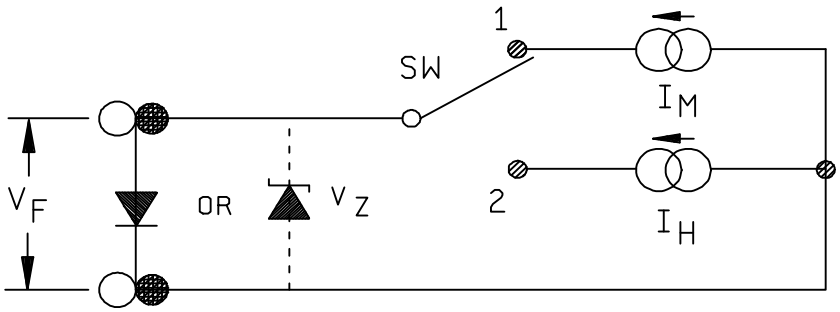
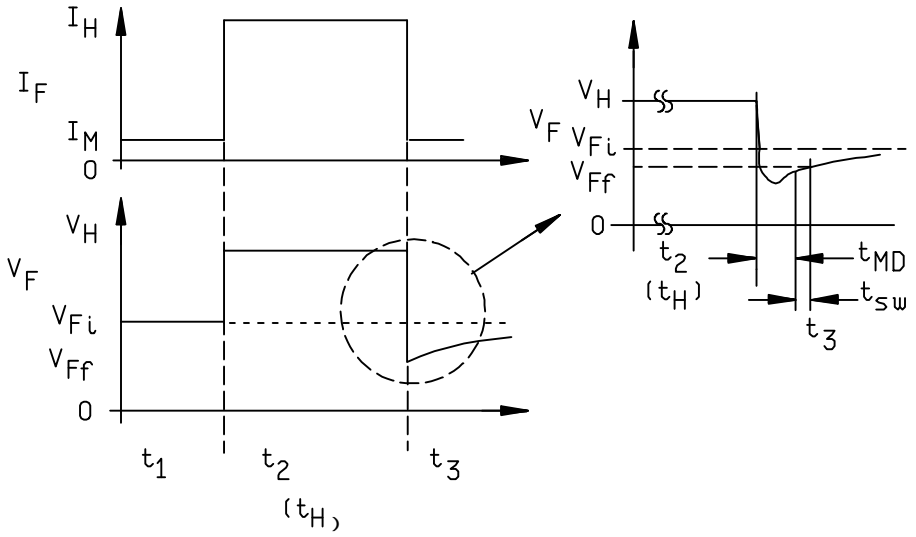


FIGURE 3101-1. Thermal impedance testing setup for diodes.

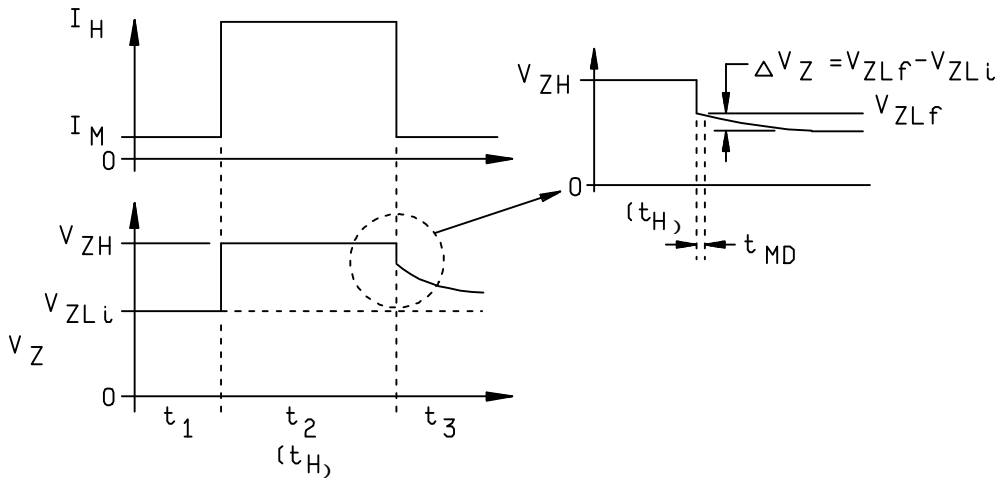
4. Test operation.

4.1 General description. The test begins with the adjustment of I_M and I_H to the desired values. The value of I_H is usually at least 50 times greater than the value of I_M. Then with the electronic switch in position 1, the value of V_{Fi} is measured. The switch is then moved to position 2 for a length of time equal to t_H and the value of V_H is measured. Finally, at the conclusion of t_H, the switch is again moved to position 1 and the V_{Ff} value is measured within a time period defined by t_{MD} (or $t_{MD} + t_{SW}$, depending on the definitions stated previously). The two current sources are then turned off at the completion of the test.



Forward biased method

FIGURE 3101-2a. Thermal impedance testing waveforms.



Zener biased method

FIGURE 3101-2b. Thermal impedance testing waveforms - Continued.

4.2 Notes.

a. Some test equipment may provide a ΔV_F directly instead of V_{Fi} and V_{Ff}; this is an acceptable alternative. Record the value of ΔV_F.

b. Some test equipment may provide $Z_{\theta JX}$ directly instead of V_{Fi} and V_{Ff} for thermal resistance calculations; this is an acceptable alternative. Record the value of $Z_{\theta JX}$.

c. Alternative waveforms, as may be generated by ATE using the general principles of this method, may be used upon approval of the qualifying activity.

*d. The zener biased method in Fig 3101-2b illustrates a positive TSP when the zener is in avalanche breakdown. It is also possible to portray a negative TSP for low voltage zeners when they are in the field-emmission or tunneling mode. A near-zero TSP can also result from these two off-setting factors of a specific operating current that must be avoided by changing to a higher or lower current. Also see paragraph 6 for TSP.

5. Acceptance limit.

5.1 General discussion. Variations in diode characteristics from one manufacturer to another cause difficulty in establishing a single acceptance limit for all diodes tested to a given specification. Ideally, a single acceptance limit value for ΔV_F would be the simplest approach. However, different design, materials, and processes can alter the resultant ΔV_F value for a given set of test conditions. Listed below are several different approaches to defining acceptance limits. The ΔV_F limit is the simplest approach and is usually selected for screening purposes. 5.3 through 5.6 require increasingly greater detail or effort. In some examples, absolute thermal impedance limits are required for correlation to surge performance such as for zeners. In such examples, setting a limit for zener diode construction with the forward biased (usual ATE) method requires prior evaluation of $Z_{\theta JX}$ (and $R_{\theta JX}$, when desired) by the zener biased method. If the zener method result is more than 10 percent higher, the limit shall be based on the more accurate zener biased measurement. In such case, if it is desired to use the forward biased method, the limit (of ΔV_F, $Z_{\theta JX}$, or $R_{\theta JX}$) shall be reduced by the extent (percentage) difference between the two methods.

5.2 ΔV_F limit. A single ΔV_F limit is practical if the K factor and V_H values for all diodes tested to a given specification are nearly identical. Since these values may be different for different manufacturers, the use of different limits is likely to more accurately achieve the desired intent. (A lower limit does not indicate a better die bond when comparing different product sources.) The diode specifications would list the following test conditions and measurement parameters:

I_H (in A)

t_H (in ms)

I_M (in mA)

t_{MD} (in µs)

t_{SW} (in µs)

ΔV_F (maximum limit value, in mV)

5.3 ΔT_J limit. (Much more involved than ΔV , but useful for examining questionable devices.) Since ΔT_J is the product of K (in accordance with 6.) and ΔV_F, this approach is the same as defining a maximum acceptable junction temperature rise for a given set of test conditions.

5.4 CU limit. (Slightly more involved than ΔT_J.) The ΔT_J limit approach described above does not take into account potential power dissipation variations between devices. The V_H value can vary, depending on chip design and size, thus causing the power dissipation during the heating time to be different from device to device. This variation will be small within a lot of devices produced by a single manufacturer but may be large between manufacturers. A CU limit value takes into account variations in power dissipation due to differences in V_H by dividing the ΔV_F value by V_H.

5.5 (K•CU) limit. (Slightly more involved but provides greater detail.) This is a combinational approach that takes into account both K factor and power dissipation variations between devices.

5.6 $Z_{\theta JX}$ limit. (For full characterization; not required for screening purposes, but preferred if the proper ATE is available.) The thermal impedance approach uses an absolute magnitude value specification that overcomes the problems associated with the other approaches. Thermal impedance is time dependent and is calculated as follows:

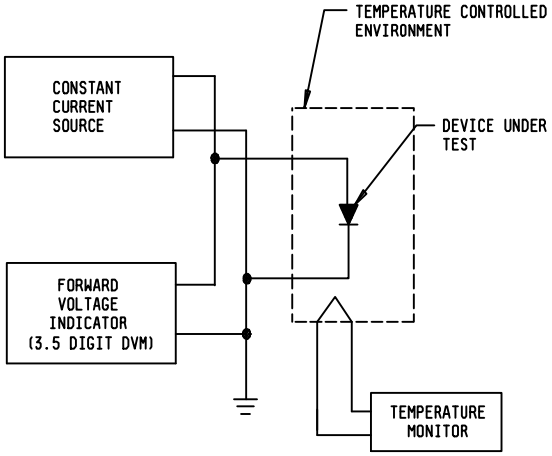
$$Z_{\Theta JX} = \frac{\Delta T_J}{P_D} = \left| \frac{(K)(\Delta V_F)}{(I_H)(V_H)} \right| {}^{O}\text{C/W}$$

5.7 $R_{\theta JX}$ limit. (For thermal resistance specification testing.) The thermal resistance to some defined point, such as the case, is an absolute magnitude value specification used for equilibrium conditions. The t_H heating time must therefore be extended to appreciably longer times (typically 20 to 50 seconds). In the example of $R_{\theta JC}$ measurements, the case must be carefully stabilized and monitored in temperature which requires an infinite heat sink for optimum results. The ΔT_J is the difference in junction temperature to the case temperature for the example of $R_{\theta JC}$.

$$R_{\Theta JX} = \frac{\Delta T_J}{P_D} = \left| \frac{(K)(\Delta V_F)}{(I_H)(V_H)} \right| {}^{O}\text{C/W}$$

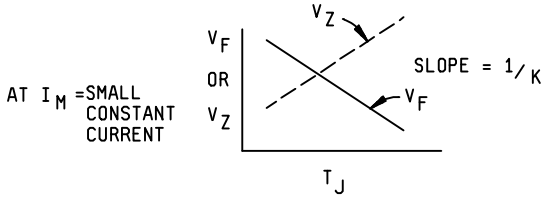
5.8 General comment for thermal transient testing. One potential problem in using the thermal transient testing approach lies in trying to make accurate enough measurements with sufficient resolution to distinguish between acceptable and nonacceptable diodes. As the diode-under-test current handling capability increases, the thermal impedance under transient conditions will become a very small value. This raises the potential for rejecting good devices and accepting bad ones. Higher I_H values must be used in this case.

*6. Measurement of the TSP V_F (or V_Z). The calibration of V_F versus T_J is accomplished by monitoring V_F for the required value of I_M as the environmental temperature (and thus the DUT temperature), and is varied by external heating. It is not required if the acceptance limit is ΔV_F (see 5.2), but is relevant to the other acceptance criteria (see 5.3 through 5.6). The magnitude of I_M shall be chosen so that V_F is a linearly decreasing function over the normal T_J range of the device. I_M must be large enough to ensure that the diode junction is turned on but not large enough to cause significant self-heating. An example of the measurement method and resulting calibration curve is shown on figure 3101-3.



Step 1: Measure V_{F1} at T_{J1} using I_M
Step 2: Measure V_{F2} at T_{J2} using I_M

Step 3: $K = \left| \frac{T_{J2} - T_{J1}}{V_{F2} - V_{F1}} \right| °C / mV$



I_M: must be large enough to overcome surface leakage effects but small enough not to cause significant self-heating.
*When using the zener direction, the I_M may also require adjustment to avoid a near zero TSP where the avalanche breakdown effects are offset by tunneling or field emission. (See 4.2, note d.)

T_J: is externally applied: (e.g., via oven, liquid) environment.

FIGURE 3101-3. Example curve of V_F versus T_J.

A calibration factor K (which is the reciprocal of the slope of the curve on figure 3101-3) can be defined as:

$$K = \left| \frac{T_{J2} - T_{J1}}{V_{F2} - V_{F1}} \right| \ ^{\circ}C/mV$$

*It has been found experimentally that the K-factor variation for all devices within a given device type class is small. The usual procedure is to perform a K factor calibration on a 10 to 12 piece sample from a device lot and determine the average K and standard deviation (σ). If σ is less than or equal to three percent of the average value of K, then the average value of K can be used for all devices within the lot. If σ is greater than three percent of the average value of K, then all the devices in the lot shall be calibrated and the individual values of K shall be used in determining device acceptance. As an alternative to using individual values of K, the manufacture may establish internal limits unique to their product that ensures atypical product removal from the population (lot-to-lot and within-the-lot). The manufacture shall use statistic techniques to establish the limits to the satisfaction of the government.

7. Establishment of test conditions and acceptance limits. Thermal resistance measurements require that I_H be equal to the required value stated in the device specifications, typically at rated current or higher. Values for t_H, t_{MD}, and heat sink conditions are also taken from the device specifications. The steps shown below are primarily for thermal transient testing and thermal characterization purposes.

The following steps describe how to set up the test conditions and determine the acceptance limits for implementing the transient thermal test for die attachment evaluation using the apparatus and definitions stated above.

7.1 Initial device testing procedure. The following steps describe in detail how to set up the apparatus described previously for proper testing of various diodes. Since this procedure thermally characterizes the diode out to a point in heating time required to ensure heat propagation into the case (i.e., the $R_{\theta JX}$ condition), an appropriate heat sink should be used or the case temperature should be monitored.

Step 1: From a 20 to 25 piece sample, pick any one diode to start the setup process. Set up the test apparatus as follows:

I_H = 1.0 A	(Or some other desired value near the DUTs normal operating current: typically higher for power diodes, and lower for zener diodes, when measured in the zener direction.)
t_H = 10-50 ms	Unless otherwise specified, for most devices rated up to 15 W power dissipation.
50 - 100 ms	Unless otherwise specified, for most devices rated up to 200 W power dissipation.
≥ 250 ms	For steady state thermal resistance measurement. The pulse must be shown to correlate to steady state conditions before it can be substituted for steady state condition.
*t_{MD} = 100 μs max	A larger value may be required on power devices with inductive package elements which generate nonthermal electrical transients; unless otherwise specified, this would be observed in the t_3 region of figure 3101-2.
I_M = 10 mA	(Or some nominal value approximately two percent, or less, of I_H.)

Step 2: Insert device into the apparatus test fixture and initiate a test. (For best results, a test fixture that offers some form of heat sinking would be desirable. Heat sinking is not needed if either the power dissipation during the test is well within the diode's free-air rating or the maximum heating time is limited to less than that required for the heat to propagate through the case.)

*Step 3: If ΔV_F is in the 15 to 80 mV range, or ΔV_{ZL} is equivalent to the same ΔT_J, then proceed to the next step. This range approximately corresponds to a junction temperature change of roughly +10°C to +50°C and is sufficient for initial comparison purposes.

If ΔV_F is less than 15 mV, return to step 1 and increase heating power into device by increasing I_H.

If ΔV_F is greater than 80 mV, approximately corresponding to a junction temperature change greater than +50°C, it would probably be desirable to reduce the heating power by returning to step 1 and reducing I_H.

NOTE: The test equipment shall be capable of resolving ΔV_F to within five percent. If not, the higher value of ΔV_F must be selected until the five percent tolerance is met. Two different devices can have the same junction temperature rise even when P_H is different, due to widely differing V_H. Within a given lot, however, a higher V_H is more likely to result in a higher junction temperature rise. For such examples, this screen can be more accurately accomplished using the CU value. As defined in 2., CU provides a comparison unit that takes into account different device V_H values for a given I_H test condition.

*Step 4: Test each of the sample devices and record the data detailed in 8.1.

*Step 5: Select out the devices with the highest and lowest values of CU or $Z_{\theta JX}$ and put the remaining devices aside.

The ΔV_F values can be used instead of CU or $Z_{\theta JX}$ if the measured values of V_H are very tightly grouped around the average value.

Step 6: Using the devices from step 5, collect and plot the heating curve data for the two devices in a manner similar to the examples shown on figure 3101-4.

*Step 7: Interpretation of the heating curves is the next step. Realizing that the thermal characteristics of identical chips should be the same if the heating time (t_H) is less than or equal to the thermal time constant of the chip, the two curves should start out the same for the low values of t_H. Non identical chips (thinner or smaller in cross section) will have completely different curves, even at the smaller values of t_H. As the value of t_H is increased, thereby exceeding the chip thermal constant, heat will have propagated through the chip into the die attachment region. Since the heating curve devices of step 5 were specifically chosen for their difference, the curves of figure 3101-4 diverge after t_H reaches a value where the die attachment variance has an affect on the device junction temperature. Increasing t_H further will probably result in a flattening of the curve as the heating propagates in the device package. If the device package has little thermal mass and is not well mounted to a good heat sink, the curve will not flatten very much, but will show a definite change in slope.

Step 8: Using the heating curve, select the appropriate value of t_H to correspond to the inflection point in the transition region between heat in the chip and heat in the package.

If there are several different elements in the heat flow path: Chip, die attachment, substrate, substrate attach, and package for example in a hybrid, there will be several plateaus and transitions in the heating curve. Appropriate selection of t_H will optimize evaluation sensitivity to other attachment areas.

Step 9: Return to the apparatus and set t_H equal to the value determined from step 8.

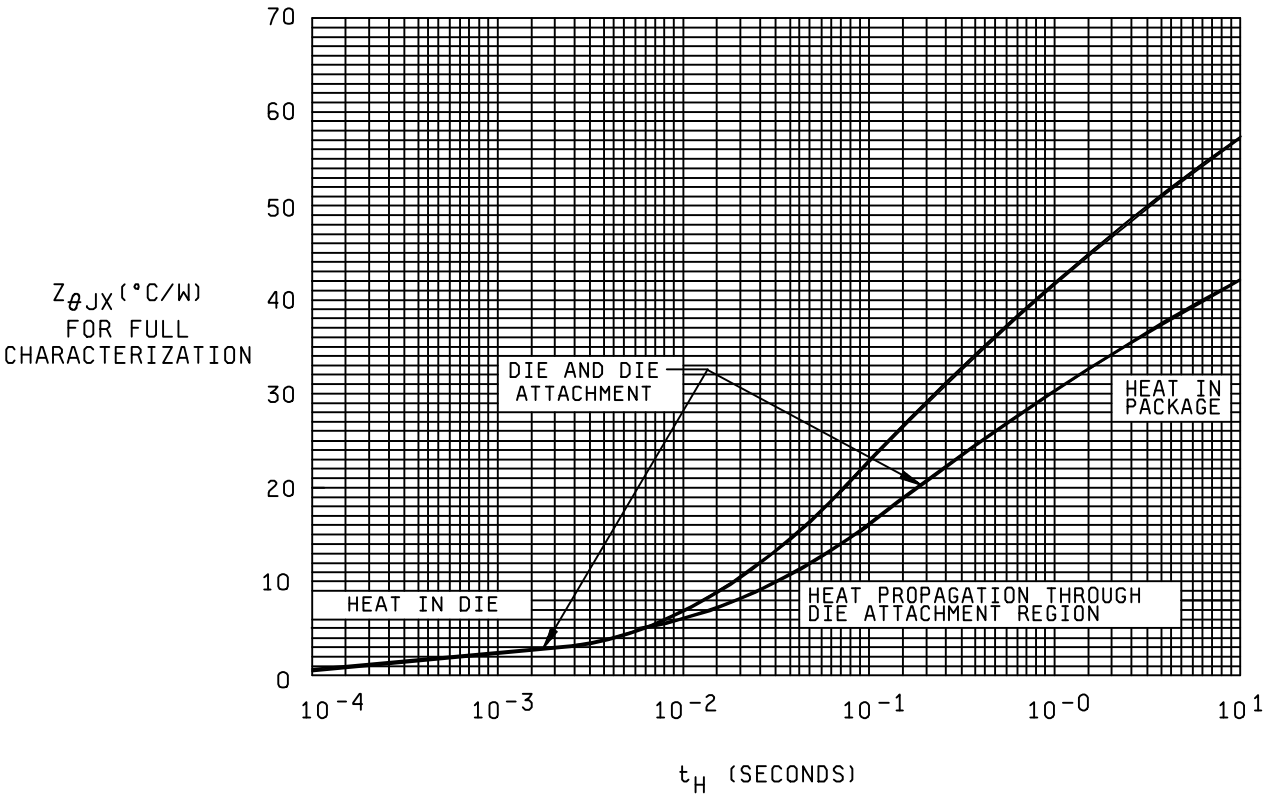


FIGURE 3101-4. Heating curves for two extreme devices.

Step 10: Because the selected value of t_H is much less than that for thermal equilibrium, it is possible to significantly increase the heating power without degrading or destroying the device. The increased power dissipation within the DUT will result in higher ΔV_F or CU values that will make determination of acceptable and nonacceptable devices much easier.

Step 11: The pass/fail limit, the cut-off point between acceptable and nonacceptable devices, can be established in a variety of ways:

a. Correlation to other die attachment evaluation methods, such as die shear and x-ray, while these two methods have little actual value from a thermal point of view, they do represent standardization methods as described in various military standards.

*b. Maximum allowable junction temperature variations between devices, since the relationship between ΔT_J and ΔV_F is about 0.5°C/mV for forward bias testing, or a measurable equivalent for zener direction testing, the junction temperature spread between devices can be easily determined. The T_J predicts reliability. Conversely, the T_J spread necessary to meet the reliability projections can be translated to a ΔV_F or CU value for pass/fail criteria.

To fully utilize this approach, it will be necessary to calibrate the devices for the exact value of the T_J to V_F characteristic. The characteristic's slope, commonly referred to as K factor, is easily measured on a sample basis using a voltmeter, environmental chamber, temperature indicator, and a power supply setup as described in 6. A simple set of equations yield the junction temperature once K and ΔV_F are known:

$$\Delta T_J = (K)\ (\Delta V_F)$$

$$T_J = T_A + \Delta T_J$$

Where T_A is the ambient or reference temperature. For thermal transient test conditions, this temperature is usually equivalent to lead temperature (T_L) for axial lead devices or case temperature (T_C) for case mounted devices.

*c. Statistically from a 20 to 25 device sample the distribution of ΔV_F or CU values should be a normal one with defective devices out of the normal range. Figure 3101-5 shows a ΔV_F distribution for a sample lot of diodes. NOTE: The left-hand side of the histogram envelope is fairly well defined but the other side is greatly skewed to the right. This comes about because the left-hand side is constrained by the absolutely best heat flow that can be obtained with a given chip assembly material and process unless a test method error is introduced. The other side has no such constraints because there is no limit as to how poorly a chip is mounted.

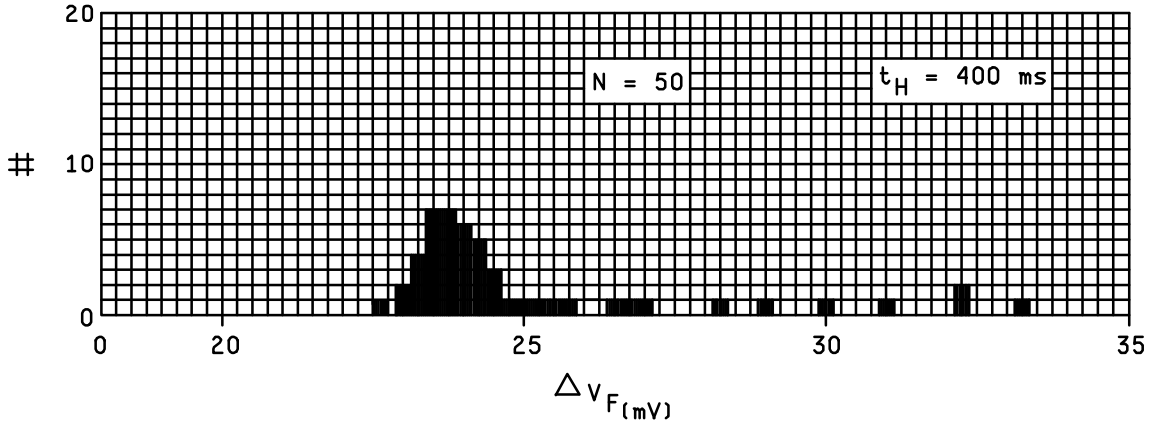


FIGURE 3101-5. Typical ΔV_F distribution.

The usual rule of thumb in setting the maximum limit for ΔV_F , CU, or $Z_{\theta JX}$ is to use the distribution average value and three standard deviations (σ). For example:

$$| (\Delta V_F) | = \overline{\Delta V_F} + X \sigma$$

high
limit

$$| (CU) | = \overline{CU} + X \sigma$$

high
limit

$$| (Z_{\theta JX}) | = \overline{Z_{\theta JX}} + X \sigma$$

high
limit

Where X = 3 in most cases and $\overline{\Delta V_F}$, $\overline{\Delta CU}$, and $\overline{\Delta Z_{\theta JX}}$ are the average distribution values.

The statistical data required is obtained by testing 25 or more devices under the conditions of step 11.

The maximum limit determined from this approach should be correlated to the diode's specified thermal resistance. This will ensure that the ΔV_F or CU limits do not pass diodes that would fail the thermal resistance or transient thermal impedance requirements.

*Step 12: Once the test conditions and pass/fail limit have been determined, it is necessary only to record this information for future testing requirements of the same device in the same package. It is also recommended that a minimum limit is established to ensure a test method error or other anomaly is investigated.

*Step 13: After the pass/fail limits are established, there shall be verification they correllate to good and bad bonded devices or the electrical properties such as surge.

The steps listed hereto are conveniently summarized in table 3101-I.

*TABLE 3101-I. Summary of test procedure steps.

General description		Steps	Comments
A	Initial setup	1 through 4	Approximate instrument settings to find variations among devices in 10 to 15 piece sample.
B	Heating curve generation	5 through 6	Using highest and lowest reading devices, generate heating curves.
C	Heating curve interpretation	7 through 9	Heating curve is used to find more appropriate value for t_H corresponding to heat in the die attachment area (for some other desired interface in the heat flow path).
D	Final setup	10	Heating power applied during t_H is increased in order to improve measurement sensitivity to variations among devices.
E	Pass-fail determination	11 through 12	A variety of methods is available such as JESD 34 for setting the fail limit; the statistical approach is the fastest and easiest to implement.
F	Verification	13	Mechanical / Electrical Correllation

7.2 Routine device thermal transient testing procedure. Once the proper control settings have been determined for a particular device type from a given manufacturing process or vendor, repeated testing of that device type simply requires that the same test conditions be used as previously determined.

New device types or the same devices manufactured with a different process will require a repeat of 7.1 for proper thermal transient test conditions.

8. Test conditions and measurements to be specified and recorded.

8.1 Thermal transient and equilibrium measurements.

8.1.1 Test conditions. Specify the following test conditions:

a. I_M measuring current ___ mA

b. I_H heating current ___ A

c. t_H heating time ___ ms

d. t_{MD} measurement time delay ___µs

e. t_{SW} sample window time ___ µs

8.1.2 Data. Record the following data:

a. V_{Fi} initial forward voltage ___V

b. V_H heating voltage ___V

c. V_{Ff} final forward voltage ___V

(NOTE: Some test equipment may provide a ΔV_F instead of V_{Fi} and V_{Ff}; this is an acceptable alternative. Record the value of ΔV_F.

Some test equipment may provide direct display of calculated CU or $Z_{\theta JX}$ this is an acceptable alternative. Record the value of CU or $Z_{\theta JX}$.

8.2 K factor calibration. (Optional for criteria 8.3a or 8.3b, mandatory for 8.3c, 8.3d, or 8.3e.)

8.3 Test conditions. Specify the following test conditions:

a. I_M current magnitude ___mA

b. Initial junction temperature ___°C

c. Initial V_F voltage ___mV

d. Final junction temperature ___°C

e. Final V_F voltage ___mV

8.4 K factor. Calculate K factor in accordance with the following equation:

$$K = \left| \frac{T_{J2} - T_{J1}}{V_{F2} - V_{F1}} \right| \ ^\circ C/mV$$

K factor ___°C/mV

8.5 Specification limit calculations. One or more of the following should be measured or calculated, as called for on the device specification (see 5.1):

ΔV_F ___mV

CU ___mV/V

ΔT_J ___°C

K•CU ___°C/V

$Z_{\theta JX}$ ___°C/W

$R_{\theta JX}$ ___°C/W