Development of Microelectronics Thermal Management Laboratory for Extreme Environments

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Abstract— **Thermal management is a critical challenge in advancing defense microelectronics, where increasing power densities and harsh environments accelerate reliability risks. Purdue Applied Research Institute, LLC (PARI) is addressing this challenge by building laboratory capabilities dedicated to thermal management in extreme environments. A central platform is a pre-configured, nine-zone, commercial thermal test vehicle (Si heater array on organic substrate), for which PARI is developing a custom controller interface to expand measurement capabilities. In parallel, PARI is designing a custom 2.5D-Si-interposer-based thermal test vehicle to probe packaging-specific challenges. As an initial demonstration, PARI will evaluate the cooling performance of additively manufactured copper cold plates. More broadly, the lab will generate data to validate finite element analysis models that provide insight into thermo-mechanical degradation mechanisms. Together, these approaches establish a foundation for assessment of next-generation cooling technologies. Leveraging Purdue University's leadership in thermal sciences, PARI seeks to bridge academia, applied research, and defense needs.**

Keywords— thermal management, advanced packaging, finite element analysis, thermo-mechanical degradation, cold plate cooling, defense microelectronics, extreme environments

I. INTRODUCTION

AI accelerators and high-performance systems increasingly concentrate power in small regions, producing local heat fluxes that challenge legacy thermal solutions. For example, Stanford demonstrated ~250 W/cm² dissipation using single-phase microchannel cooling, and up to ~800 W/cm² under more aggressive conditions on a 52 mm² footprint [1]. In more extreme demonstrations, Goodson's group showed that micro-coolers can remove ~1,000 W/cm² with modest temperature rise [2]. Meanwhile, evolving cooling schemes leveraging capillary evaporation have achieved > 600 W/cm² in experimental setups [3]. These trends imply that local power densities on the order of 2.5 to 10 W/mm² (or more in hotspots) may be realistic in advanced accelerator packages. Such levels far exceed the envelope of conventional test benches and pose new challenges for packaging and cooling technologies.

For the Department of War (DoW), the challenge is amplified: in addition to managing extreme heat flux, advanced computing and autonomous systems must be ruggedized for deployment in fielded platforms, surviving wide thermal cycles, vibration, shock, and radiation exposure. DARPA's Miniature Thermal (Minitherms3D) initiative is advancing compact, high-performance thermal architectures for 3D stacked electronics, aiming to support multi-kilowatt stacks in constrained volumes [4]. Likewise, DoD Directive 3000.09 requires autonomous systems to undergo rigorous validation and operational testing in realistic environments to ensure mission reliability and robustness [5]. These programs underscore the need for thermal testbeds that bridge performance and ruggedization.

II. EXPERIMENTAL PLATFORMS AND METHODS

The laboratory buildout at PARI is centered on developing versatile thermal test vehicles to probe advanced packaging challenges under extreme environments. The first capability is based on a commercial nine-zone thermal test vehicle (Si heater array on organic substrate). This platform enables baseline cooling evaluations. A custom controller interface is under development to extend its flexibility, enabling programmable heating profiles and multi-zone operation beyond the commercial specification.

In parallel, PARI is pursuing a custom thermal test vehicle based on a 2.5D Si-interposer architecture. This testbed integrates multiple thermal test chiplets of varying sizes (3×3 mm, 9×9 mm, and 9×21 mm) onto a silicon interposer with redistribution layers and through-silicon vias. This vehicle is intended not only for empirical testing but also as a platform for validating finite element thermo-mechanical models, including simulations of interconnect reliability, warpage, and chiplet-to-chiplet thermal interactions. The interface and custom controller used with the TEA test vehicle developed in

To support these validation efforts, the lab has invested in infrared thermal imaging for high-resolution surface temperature mapping and a white-light profilometer for quantitative warpage measurements. These tools enable direct comparison of experimental data with model predictions, strengthening confidence in FEA-based reliability assessments.

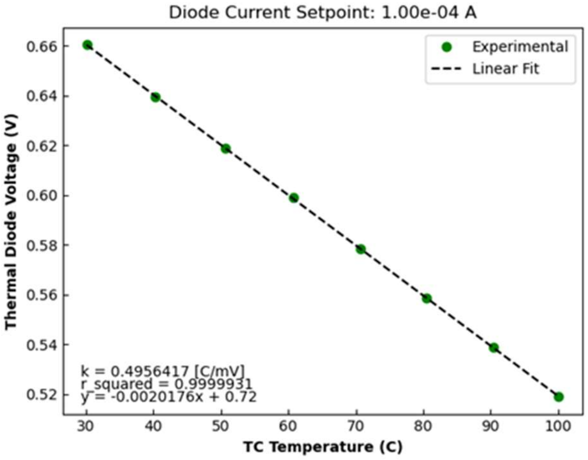
In addition to structural packaging elements, the laboratory is also intends to evaluate performance of thermal interface materials (TIMs). Both steady-state and transient tests can be performed to measure thermal resistance and conductivity, while environmental cycling experiments allow monitoring of degradation mechanisms such as pump-out, delamination, and interfacial cracking. Where appropriate, JEDEC-style accelerated stress tests (e.g., thermal cycling, high-temperature storage, and power cycling) can be employed to establish benchmarks aligned with industry and defense standards for reliability.

As an initial demonstration, PARI will evaluate the cooling performance of student-designed, additively manufactured copper cold plates in collaboration with academic and industry partners. This study serves as a representative application of the new test capabilities while generating datasets to benchmark cooling solutions against validated models. By combining flexible hardware with advanced diagnostics, TIM characterization, and standardized reliability testing, the laboratory establishes a foundation for assessing next-generation thermal management technologies and their performance under conditions representative of defense applications.

III. PRELIMINARY EXPERIMENTAL RESULTS

Preliminary experiments were conducted to validate temperature sensing, control, and diagnostic capabilities that underpin the thermal test platforms described in Section II. Initial efforts focused on establishing accurate and repeatable temperature measurements, followed by system-level demonstrations of scalable sensing and thermal mapping.

To establish measurement fidelity, a single thermal test chip (TTC) was wirebonded to a ceramic chip carrier and placed in a controlled furnace environment with an embedded thermocouple reference. The forward voltage of on-die temperature sensing diodes was measured across a temperature sweep from 30 °C to 100 °C. Measurements were performed using both a benchtop precision constant-current source and a commercial constant-current integrated circuit intended for use in the custom controller. The resulting calibration curves exhibited highly linear behavior across the full temperature range, with closely matched K-factors between the two biasing approaches. These results confirm that the IC-based current source provides accuracy comparable to laboratory instrumentation, enabling scalable integration into multi-zone thermal test vehicles (Fig. 1).



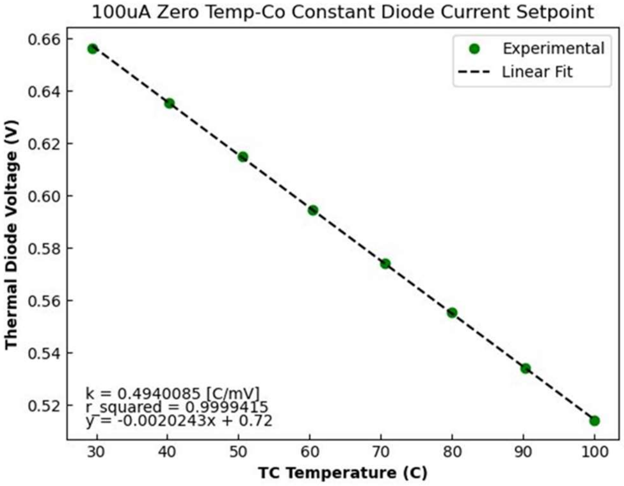


Fig. 1. Calibration plots of TTC diode forward voltage versus temperature from 30 °C to 100 °C, comparing benchtop constant-current biasing to an IC-based constant-current source. Linear fits demonstrate consistent K-factors across both approaches.

Beyond single-device calibration, the performance of the custom temperature measurement and power controller architecture was evaluated. The ADC and multiplexer chain successfully scanned all sixty-plus diode sensors in under one second, demonstrating that high-channel-count temperature acquisition can be performed in near real time. The controller architecture, shown schematically in Fig. 2, is explicitly designed to scale from the nine-zone commercial TTV to the higher channel densities anticipated in the custom 2.5D Si-interposer-based thermal test vehicle, providing a unified sensing and control framework across platforms.

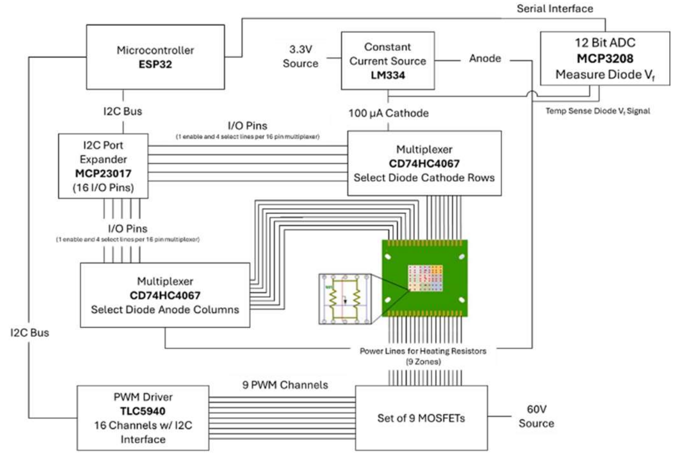


Fig. 2. Block diagram of the custom temperature measurement and power control architecture, illustrating diode biasing, multiplexing, ADC acquisition, and controller integration.

Thermal mapping experiments were also performed under representative boundary conditions. Multi-zone heating configurations were applied to the commercial TTV, and surface temperatures were recorded using infrared thermal imaging. A representative thermogram is shown in Fig. 3, highlighting spatial temperature gradients under non-uniform power dissipation. These measurements were compared against embedded diode telemetry to assess spatial resolution and consistency between sensing modalities. The combined dataset demonstrates the ability to resolve thermal gradients across the device and highlights the value of distributed sensing for characterizing realistic operating conditions.

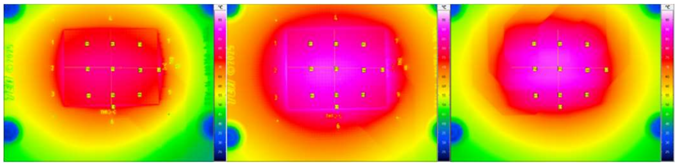
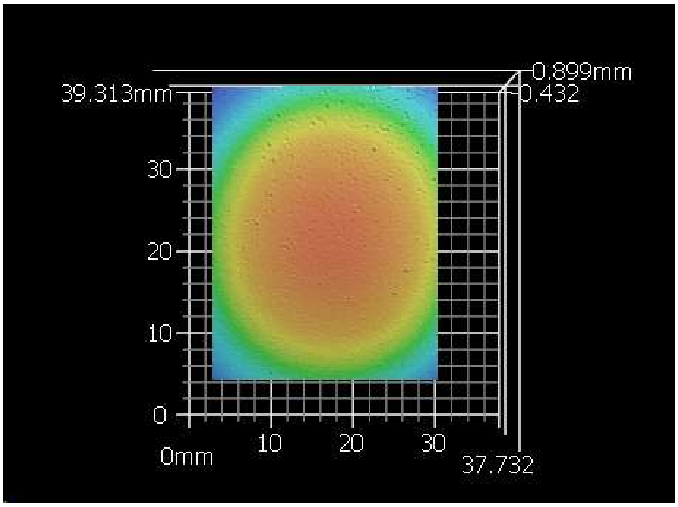


Fig. 3. Collage of infrared thermal image of the commercial nine-zone thermal test vehicle under multi-zone heating, illustrating non-uniform temperature distribution across the die surface.

In parallel, initial out-of-plane deformation measurements were conducted using white-light profilometry. Warpage was measured under unpowered conditions, during steady-state heating, and following cooldown. Figure 4 shows a representative height map measured during powered operation, revealing measurable curvature induced by thermal loading. These results underscore the coupling between thermal gradients and mechanical response, providing critical experimental inputs for subsequent thermo-mechanical modeling and reliability analysis.



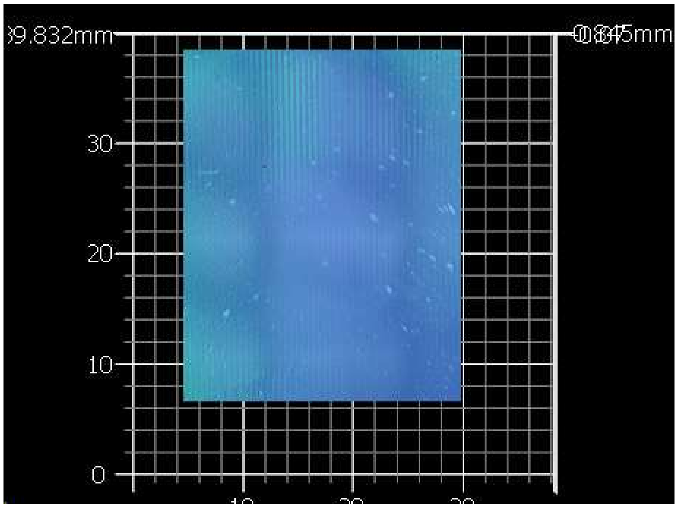


Fig. 4. White-light profilometry height maps of the thermal test vehicle under zero applied current (top) and steady-state heating in adjacent zones (bottom), showing thermally induced out-of-plane deformation.

Together, these preliminary results validate the accuracy, scalability, and multi-modal diagnostic capability of the laboratory infrastructure, establishing readiness for more advanced studies of cooling solutions, thermal interface materials, and package-level reliability.

IV. MODELING AND ANALYSIS

A central objective of the laboratory is to generate experimental datasets that directly support the development and validation of finite element (FE) models for advanced microelectronics packaging. The combination of embedded temperature sensing, infrared thermal imaging, and profilometry enables controlled comparison between measured responses and model predictions across thermal and thermo-mechanical domains.

To accomplish this goal, multiple models were created across several domains to bring the TTV into the digital realm for modeling, simulation, and analysis. A simplified process flow that shows the process leveraged for creation of the FE models is shown in Fig 5.

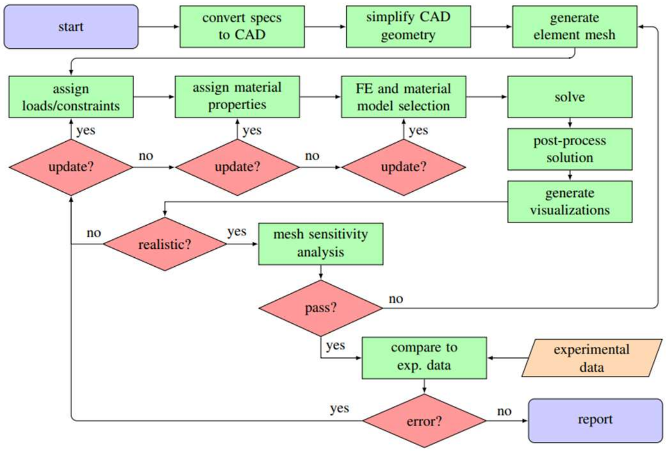


Fig. 5. Simplified FE modeling workflow

To realize the process of bringing the TTV into the digital realm, data was extracted by both measurement and vendor supplied data to generate a three-dimensional parametric, boundary representation (B-REP) model [7]. A top view showing the TTV in both the physical realm, and the realized digital realm can be seen in Fig 6. For reader clarity, the small regions depicted within the die shown in the right image represent experimental thermal measurement diode locations within the TTV.

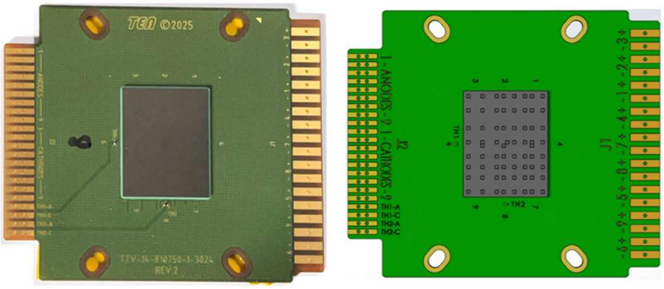


Fig. 6. Thermal Test Vehicle (left) and TTV B-REP model (right).

To ensure adequate hardware resources were available to perform the selected linear transient heat transfer analysis solution, two discretization simplifications were employed: a) a local subsection of the package thermal responses were simulated, and b) symmetry was employed. Two approaches for symmetrical loading were considered: half-symmetry (not shown), and quarter symmetry, as seen in Fig 7. Multiple thermal zone-loading scenarios were considered for all simulated cases.

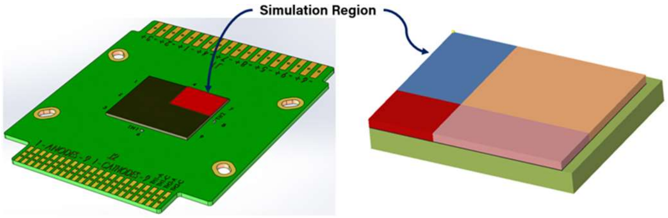
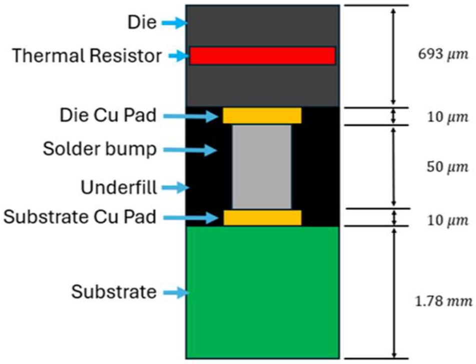


Fig. 7. TTV Geometric model showing domain of interest (left) and discretized, quarter-symmetry, FE solution domain (right)

Each solder interconnect was discretized explicitly, as opposed to using a rule-of-mixtures approach to model the solder interconnect region [6]. Cross-section details for the individual interconnects can be seen in Fig 8. The quarter-symmetry implementation resulted in a total of 15,279,610 degrees of freedom (DOFs) as shown in Table 1. Future efforts will focus upon the study of the reduction of the number of DOFs to reduce solution times and expand random access memory (RAM) availability [8].



NOTE: NOT TO SCALE

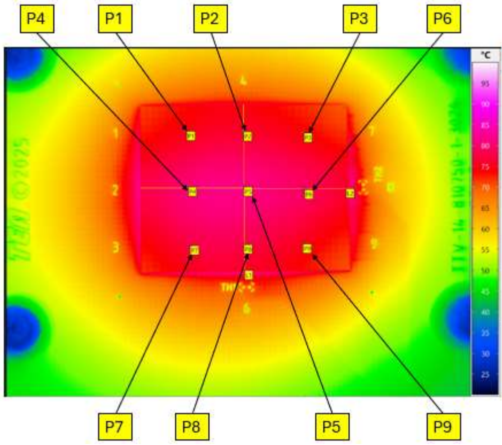
Fig. 8. Solder interconnect cross-section detail)

Table 1. FE Simulation Model Solution Approach Times

FE Model	Substrate	Symmetry	DOFs	CPU Threads [n]	Wall Clock [h:m:s]	Total Time [h:m:s]
TTC Chiplet	Section Local	None	78,409	8	00:03:14	00:01:15
Single Zone	Section Local	None	6,988,132	20	02:55:05	01:20:19
TTV	Full PCB	None	---	---	---	---
TTV	Chip, Local	None	61,004,395	---	---	---
TTV	Chip, Local	Half	30,559,219	20	09:25:17	03:35:07
TTV	Chip, Local	Quarter	15,279,610	20	03:41:24	01:11:50

The overarching goal of the experimental test – modeling effort is to predict local stress distributions and strain behaviors induced by coefficient of thermal expansion (CTE) mismatches to gain a better understanding of what a simulated system might experience with respect to reliability degradation. It's important to note that accurate thermal model performance is critical when considering thermal-induced mechanical stress due to mechanical warpage.

Thermal models are used to predict heat spreading, temperature gradients, and boundary-condition sensitivity under applied power. Experimental calibration data from diode-based temperature sensors, as seen in Fig 6, provide a baseline for validating modeled temperature fields, while infrared thermography enables spatial comparison of surface temperatures. An example comparison between simulated and measured temperature distributions is shown in Fig. 8, illustrating reasonable agreement in both magnitude and spatial trends. It should be noted that the FE results were obtained using model symmetry, whereas the experimental tests conducted exhibited some asymmetry. With that said, the result correlations were considered reasonable on the die face.



ID	Exp Avg	FE
P1	74.86	77.7
P2	76.01	77.7
P3	74.15	77.7
P4	80.49	80.0
P5	81.16	80.0
P6	78.95	80.0
P7	77.38	77.7
P8	77.64	77.7
P9	75.30	77.7

Fig. 8. Comparison of simulated and experimentally measured surface temperature distributions for a representative 80C (zones 2-5-6) heating condition.

Quantitative results showing transient thermal loading and simulated responses can be seen in Figure 9. It should be noted that the thermal dwell-time chosen was for model exercise and demonstration purposes. While the simulated responses appear to approach steady-state behavior, the dwell time would need to be increased to better understand thermal behavior on regions such as the back side of the AP substrate.

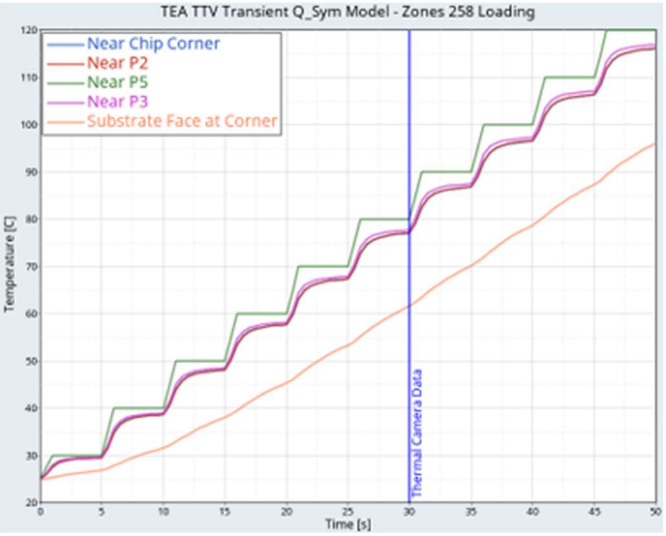


Fig. 9. Transient thermal test loading ramp-up and simulated responses.

Beyond thermal behavior, the laboratory places particular emphasis on thermo-mechanical degradation mechanisms that emerge under high power density operation. Key areas of focus include solder joint fatigue driven by cyclic thermal loading, delamination at die, substrate, or thermal interface material (TIM) interfaces, and global or local warpage of interposers and organic substrates. Results derived from FE thermal modeling are currently being used as load inputs to drive mechanical warpage models for qualification against profilometer-based deformation measurements while under thermal load.

In addition to strains induced by mechanical warpage models, thermal interface materials are in the process of being incorporated explicitly into both experimental testing and modeling workflows. Steady-state and transient measurements are expected to provide effective thermal resistance data, while JEDEC-style accelerated stress conditions enable observation of degradation mechanisms such as pump-out and interfacial separation. The whole of these results are intended to inform future modeling efforts to increase information regarding long-term performance and reliability aspects of novel advanced packaging technologies.

By closing the loop between experiment and simulation, the laboratory is working towards establishing a framework for validated, predictive modeling of advanced cooling and packaging architectures to better understand current and future AP technologies. This approach also serves as a mechanism to enable a more holistic assessment of emerging technologies—such as additively manufactured cold plates and heterogeneous interposer-based designs—prior to integration into fielded systems.

V. DISCUSSION AND RELEVANCE

The results presented demonstrate the establishment of a scalable experimental and analytical framework for evaluating thermal management technologies under conditions relevant to advanced defense microelectronics. Unlike traditional test approaches that emphasize either performance or reliability in isolation, the PARI laboratory integrates high-power thermal testing, multi-modal diagnostics, and validated modeling to address both simultaneously.

This capability is directly aligned with the Department of War's need to transition high-performance computing and autonomous systems from controlled datacenter environments into operational platforms. In such settings, cooling solutions must not only manage extreme heat flux but also maintain reliability under wide thermal excursions, vibration, and other environmental stresses. The experimental results presented in Sections III and IV demonstrate how package-level thermal and mechanical responses can be quantified and incorporated into predictive models.

Equally important, the integration of experimental data with validated FEA models enables quantitative extrapolation beyond specific test cases. This approach supports down-selection of cooling technologies, assessment of packaging risk, and prediction of lifetime performance under mission-relevant conditions.

Embedded within Purdue University's broader ecosystem of thermal sciences and microelectronics research, PARI's laboratory is positioned to bridge fundamental advances with applied research and technology transition. The laboratory is open to collaboration with government sponsors, industry partners, and academic groups seeking to advance the performance and ruggedization of thermal management technologies for defense applications.

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