Thermal Test Vehicle for Transient Thermal Characterization of Large Body Size Chips

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Abstract

Thermal management is becoming an ever more critical challenge for high performance computing (HPC) chips as the power density and chip size increase. For heterogeneous integration with multiple chiplets and very large body size in the package, the characterization of the thermal behavior becomes even more challenging. This paper describes a design practice using Thermal Test Chips (TTC) and Thermal Test Vehicles (TTV) which can accurately emulate the heating power distribution of a real functional chip, providing the capability for configurable power distribution and in situ temperature measurement on the chip. The TTC on the TTV features a design incorporating an array of heating zones, each equipped with in situ temperature-sensing diodes. With the array design of the TTV, we can configure the heating zones to our preference, thereby simulating either uniform heating or "hot spots". Various test items can be measured based on a flip chip ball grid array (fcBGA) TTV integrated with a liquid cooled cold plate in accordance with the TTV design. By utilizing the temperature sensing diodes situated at various points throughout the TTC, we can ascertain the comprehensive temperature distribution (transient and steady state) across the TTC. Furthermore, the transient thermal characterization can be performed by selecting specific sensing diodes to obtain the thermal impedance (Zth) curve and structure function. The thermal resistance from junction to case (θ_{JC}) and from junction to ambient (θ_{JA}) can also be characterized under different conditions of thermal interface materials (TIMs) and coolant flow rates. Based on various experimental results, we have demonstrated that the TTV design is suitable for the thermal characterization of large-body-sized chips. It will be useful for a comprehensive and in-depth understanding of the on-die and package level heat dissipation behavior, which can be used for characterization and optimization of real-chip thermal performance.

Nomenclature

HPC	high performance computing
TTC	thermal test chip
TTV	thermal test vehicle
TIM	thermal interface material
θ_{JA}	thermal resistance between junction to ambient, °C/kW
θ_{JC}	thermal resistance between junction to case, °C/kW
fcBGA	flip-chip ball grid array
T_j	junction temperature, °C
T_{amb}	ambient temperature, °C
BLT	bond line thickness, um
Z_{th}	thermal impedance, °C/kW

1. Introduction

High performance computing (HPC) is finding increasing use in the areas of artificial intelligence (AI), machine learning, IOT (Internet of Things), and so on. As the manufacturing process nodes of chips become more advanced and the transistor density increases, the power density of chips also becomes significantly higher. The heterogeneous integration with multiple chips of various functionalities, sizes, and power distributions all in the same package is widely used. Consequently, HPC systems generate a substantial amount of heat, which, if not dissipated effectively, can result in thermal stress and damage to the semiconductor device. At the same time, the characterization of the thermal behavior, which is necessary for developing effective thermal management solutions, becomes even more challenging. Effective tools and capabilities are needed to develop thermal management solutions to safeguard the performance of the semiconductor device.

Thermal Test Chips (TTC) and Thermal Test Vehicles (TTV) are great tools for thermal characterization, and such tools can provide the early stage thermal design directions while the chip is under development. To accommodate a wide variety of applications, the Unit Cell concept is used which is the basic building block for the TTCs. Each Unit Cell consists of a heating resistor and an embedded diode temperature sensor. By using multiple Unit Cells in a square or rectangular array configuration, it is possible to approximate almost any size application chip. [1]

Flip chip ball grid array (fcBGA) packages are predominantly utilized for HPC application chips, particularly for heterogeneous integration of multiple chiplets. For thermal characterization, both the overall heat dissipation performance and the characterization of "hot spots" are essential, owing to the non-uniform heat generation from the various chip cores or chiplets. As the power density of chips increases, air is becoming a less viable medium for heat removal. Instead, the industry is now looking towards circulating a liquid coolant, with a heat capacity superior to air, to more effectively remove heat from those high power chips. [2]

Thermal interface materials (TIMs) are thermally conductive materials extensively employed in semiconductor packaging to reduce the thermal contact resistance caused by air gaps between the cooling solution and the chip dies. The

TIM is situated between the TTC die surface and the liquid cooling plate. A precise pressure from the cooling plate is essential for optimal contact with the TIM.

To demonstrate the TTV design as an effective tool for thermal characterization of HPC chips, we performed testing using a selection of standard test items. In this paper, we assess the θ_{JC} and θ_{JA} of the TTC by applying a uniform heating power over the TTC die. The structure functions were assessed using the designated sensing diode on the TTC, in accordance with the transient temperature curve. The θ_{JC} measurement methodology adheres to the dual-interface technique outlined in JEDEC JESD51-14. [3] θ_{JA} in this paper represents the thermal resistance between the junction and the coolant, with the coolant temperature set to 25 ℃ for our measurement. Non-uniform heating measurement will be the subject of further study.

2. Thermal test vehicle and package design

2.1 Thermal test chip (TTC) Unit Cell

The TTCs must be able to closely approximate the power input and power density distribution of the application chip, and simultaneously accurately sense the temperature distribution (using integrated sensors) over the entire die (with resolution down to 1mm x 1mm), in real-time. [4]

We used the thermal test chip which is based on a 1mmX1mm silicon Unit Cell and is designed to provide maximum flexibility for thermal characterization of semiconductor packages. Unit Cells can be used in a square or rectangular array. An integrated center diode temperature sensor in each Unit Cell enables temperature measurements to be made in multiple locations in any array configuration. [5]

Each Unit Cell is equipped with a resistor of nominal value 10.5 ohms and a temperature sensing diode. Both the heating resistor and the sensing diode are individually accessible, allowing both heating and temperature measurement as shown in Fig.1. The resistor covers >69% of die area and can be accessed with wire bonding or bump pads. [6]

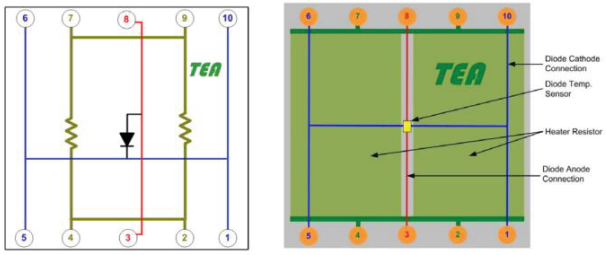

Fig.1. Unit Cell electrical representation and layout

2.2 TTC configuration

Thermal test chips have become extensively utilized in the qualification of package designs. In our study, we designed a bare die TTC with dimensions of 32mm x 27mm x 0.7mm (L x W x H). The TTC comprises an array of 5 x 5 heating zones, with each zone featuring an array of 5 x 6 Unit Cells as shown in Fig. 2. The TTC has Cu pillars with lead-free solder cap, with 0.2mm pitch.

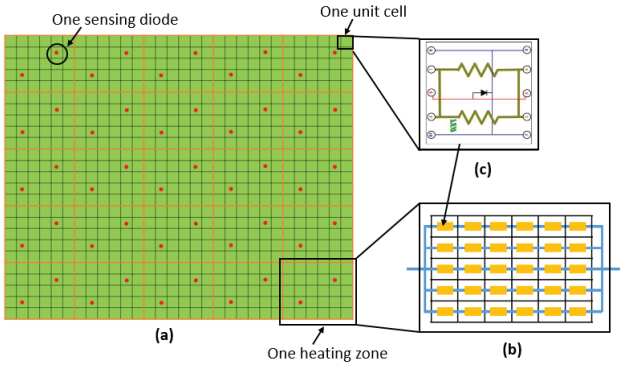

Fig. 2. One TTC (a) contains 5 x 5 heating zones (b), and one heating zone contains 5 x 6 Unit Cells (c)

In order to configure the power zones for the desired power distribution for the chip, in each heating zone, six Unit Cells are initially arranged in series, after which five identical configurations are connected in parallel to create a 5x6 matrix. The 25 heating zones are not interconnected, allowing each to be accessed and controlled directly and individually. This design affords the flexibility to connect them in series or in parallel, depending on the desired connection topology.

Up to 750 diode sensors can be available in each TTC. In this design, only two sensing diodes are routed out, making them accessible in each heating zone. The routed-out sensor locations are indicated by the red dots shown in Fig. 2 (a). With a total of 25 heating zones, there are 50 sensing diodes evenly distributed across the TTC.

2.3 Thermal test vehicle design

A flip chip thermal test vehicle was developed to evaluate the thermal performance of the package. For this particular TTV, we included eight additional TTC dies (not shown) encircling the central main TTC on the TTV to replicate the heterogeneous package configuration for various functional dies, as is typical of GPUs in the market. In this paper, we concentrate exclusively on the measurement of the central main TTC marked in Fig. 3 (and described in Section 2.2). Further investigation and discussion regarding the surrounding dies will be undertaken in future studies.

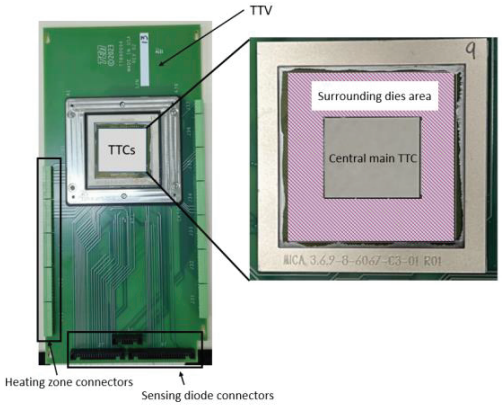

Fig. 3. The view of the TTV

For TTV assembly, the TTC is attached to an organic substrate using flip chip and is then underfilled. It is then assembled onto the PCB (printed circuit board) using ball grid array (BGA). Each heating zone and sensing diode is routed out through the TTV substrate to the individual connectors on the PCB.

The cross-sectional view of the fcBGA package together with TIM and the cooling plate is shown in Fig. 4. From the top to the bottom is the cooling plate, the TIM layer, the silicon TTC, a layer of underfill around solder bumps, an organic substrate, an array of solder balls, and finally the TTV test board (PCB). The aim of this design is to more precisely replicate the actual application of an HPC chip, with the bare die affixed to the substrate using bumps and UF (underfill) epoxy, and the substrate is then mounted onto an application board (PCB) using solder balls. The pressure applied by the cooling plate can be finely adjusted through the use of spring-loaded screws designed for fixation.

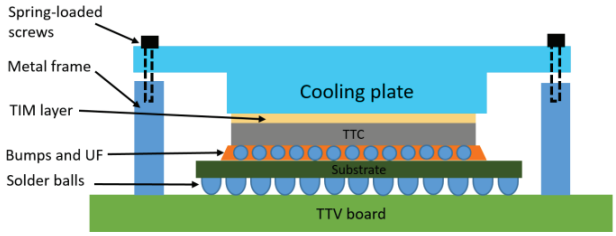

Fig. 4. The cross-section view of the TTV system

2.4 Liquid cooling

The direct-to-chip liquid cooling system hinges on circulating a fluid through a cooling plate heat exchanger located directly on the chip. The liquid cooling plate is affixed and makes contact with the top surface of the TTC using a TIM to transfer heat from the TTC to the circulating coolant. The cooling plate's surface is composed of copper, and the heat dissipated from the chip is absorbed into the coolant loop. The heated fluid is then circulated through a large liquid tank which is temperature controlled.

The cooling plate is secured to a rectangular metal frame by four spring-loaded screws at the corners of the frame, as depicted in Fig. 4. The spring-loaded screw is a fastener equipped with a spring, which maintains a consistent pressure by compressing the spring when the screw is tightened into position. With a torque wrench, we can attain the target torque on the spring-loaded screws, thereby ensuring that a consistent pressure is applied to the TTC. The applied pressure can be adjusted by altering the torque setting of the torque wrench.

The coolant employed in our experiment consists of a blend of 75% DI (deionized) water and 25% propylene glycol to simulate a common commercially used coolant on the market. The temperature of the coolant is regulated by a heater and a refrigeration unit within the tank. A temperature sensor positioned at the inlet of the cooling plate continuously monitors the coolant's temperature to ensure precise control. A valve and a flow rate meter are also incorporated into the coolant loop to regulate and oversee the coolant's flow rate.

2.5 Thermal interface material (TIM)

An efficient TIM is essential for optimal heat dissipation performance throughout the TTC to the cooling plate. For our TTV design, a layer of TIM is attached between the TTC top surface and the liquid cooling plate.

Fig. 5. Thermal interface material between interfacing surfaces

Given the surface roughness of both the silicon die and the cooling plate as shown in Fig. 5, there may be microscopic gaps that could trap air. Direct contact between the cooling plate and the TTC might not achieve optimal thermal dissipation; thus, employing a TIM is better for heat dissipation performance. An appropriate pressure can enhance the contact between the TIM and the TTC and facilitate superior heat dissipation. This pressure is exerted by the spring-loaded screws attached to the cooling plate.

In our study, both configurations (with TIM and without TIM) were evaluated to extract the θ_{JC} value by the dual interface method specified by JESD51-14 .

3. Experimental setup

3.1 Heating and sensing

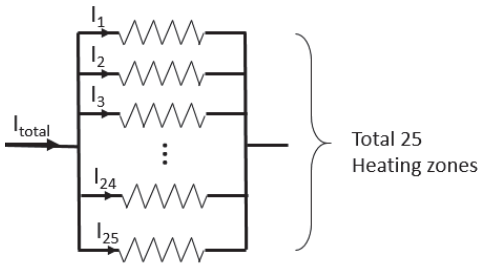

Fig. 6. Connection of heating zones

Given that the resistance of each heating zone is nearly identical, we can connect 25 heating zones all in parallel as shown in Fig. 6. By utilizing a constant power provided by an external power supply, we can achieve uniform heat distribution within the TTC.

In the TTC design, a total of 50 sensing diodes offer remarkable flexibility and spatial resolution. We can measure the transient temperature curve and structure function based on the selected sensing diodes. As a small current traverses the diode, the voltage drop across its terminals exhibits a linear dependency on temperature. Consequently, before heating the TTC, the diode was calibrated in an oven (or oil bath) to determine its voltage response as a function of temperature.

3.2 Measurement configuration

The coolant is maintained at a constant temperature of 25°C throughout, from before the heating phase until its

conclusion. As it interacts with the TTC through the cooling plate, the initial temperature of the TTC is also closely aligned with this temperature.

The θ_{JA} can be assessed through the thermal steady-state condition based on the TTC design. It is determined using the junction temperature (T_j) during the thermal equilibrium, the ambient temperature (T_{amb}), and the applied heating power (P_H), with the formula below. T_{amb} is the coolant inlet temperature, which is set to 25 ℃ in our experiment. We can effortlessly measure the voltage on each sensing diode during the thermal equilibrium, thereby ascertaining the temperature distribution map across the entire TTC. The θ_{JA} of the package is calculated using the maximum T_j across the TTC. Given uniform heating, the temperature in the central area is typically elevated compared to the sides and corners of the chip, due to the heat spreading effect. Hence, the T_j of the central sensor is used for θ_{JA} calculation.

$$\theta JA = \frac{T_j - T_{amb}}{P_H}$$

For θ_{JC} measurement, we applied the transient thermal measurement approach with a commercially available test system to analyze the structure function of the devices and the Zth curve for the selected sensing diodes. The overall test setup is shown in Fig. 7.

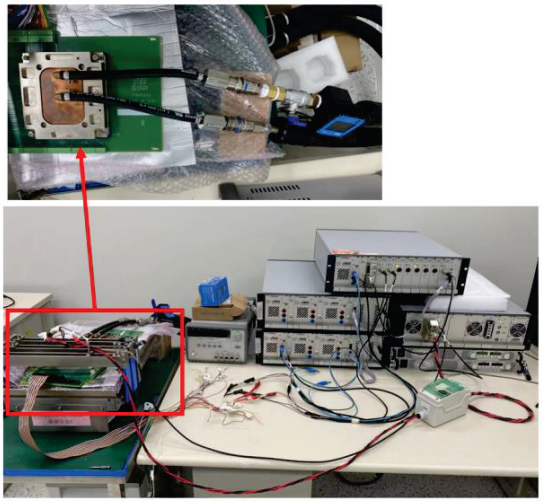

Fig. 7. θ_{JC} test setup

The θ_{JC} is a measure of the ability of a semiconductor device to dissipate heat from the TTC die junction to the surface. [7] Two measurements were obtained for each chosen diode: one without TIM and the other with TIM. Each measurement was converted to structure function and Zth curve using the Network Identification by Deconvolution (NID) method, and the corresponding measurements were compared to each other. With this method, we can get the θ_{JC} using a similar approach to the JEDEC JESD51-14 dual interface method. [7]

The measurement employs the transient method in accordance with the JESD51-14 standard to get the structure function, which entails recording the temperature transient curve during the cooling period. Prior to capturing the curve, the temperature of the TTC junction must be elevated to a reasonably higher temperature at thermal equilibrium. With the structure function, we can have more comprehensive data for subsequent simulation and design.

4. Results and discussions

4.1 TTC heating

The design of the TTV provides significant flexibility in connecting TTC heating zones either in series or in parallel to simulate varied heat distributions across the TTC.

Firstly, the TTC was powered with a small power of 20W to assess the temperature distribution across its surface without a TIM and a cooling plate, while utilizing a FLIR (Forward Looking Infrared) camera to monitor the surface temperature of the TTC, as depicted in Fig. 8. Nine reference markers were established to measure the temperature at the edges, the corners, and the center. The temperatures recorded by FLIR from Markers No.1 to 9 are 41.4, 42.2, 39.9, 42.1, 43.9, 41.9, 41.2, 43.4, and 42.4 ℃, respectively. There is approximately a 4°C variation among the different locations. The primary reason lies in the varying heat dissipation conditions across different areas of the TTC. The corners exhibit the most favorable heat dissipation conditions due to lateral heat spreading.

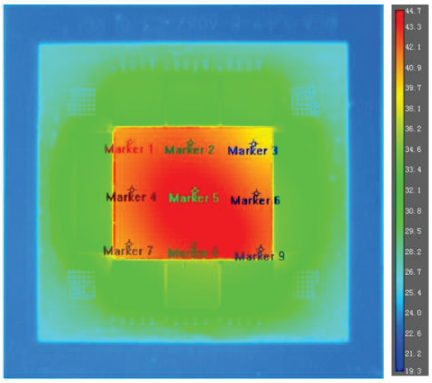

Fig. 8 TTC surface temperature heated by 20W power without TIM and a cooling plate

By connecting the heating power across various zones, we can also effectively simulate “hot zones” as shown in Fig. 9. Connecting only a single heating zone — whether central, corner, or side — and heating it with minimal power, without employing TIM or a cooling plate, we can see the temperature distribution with FLIR..

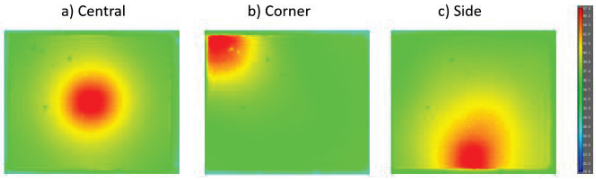

Fig.9. a) heating zone at central, b) heating zone at corner, c) heating zone at side.

In this paper, we focus on uniform heating for thermal resistance characterization.

4.2 Sensor temperature and θ_{JA} measurement

The temperature distribution across the TTC is crucial for assessing the overall thermal performance. The temperature value of each sensing diode can be ascertained by simply measuring the voltage across the sensing diode at the thermal steady-state. Fig. 10 illustrates an example of sensor temperature measurements at both the central and corner positions, with a uniform heating power of 300W applied with TIM. The coolant flow rate is maintained at 2.0 L/min. The T_j recorded by the central diode is 40.4°C, while the corner sensor registers 35.8°C. The temperature distribution of the entire TTC under varying conditions will be the subject of future investigation. Here in this paper, we concentrate on the TTV design concept, which has been demonstrated to be advantageous for our continued research. Based on the formula delineated in Section 3.2, we can readily determine the θ_{JA} value of the package from the measured T_j of the central sensor.

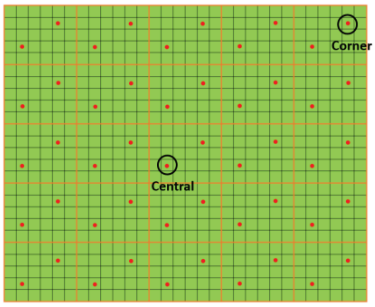

Fig. 10. Sensing diodes at central and corner for temperature measurement.

4.3 θ_{JC} measurement

To prove the TTV design concept as the first step, the diode situated in the central area (as shown in Fig. 10) was chosen for the transient thermal characterization of the θ_{JC}. This choice is predicated on its ability to minimize heat flow in the horizontal orientation while exhibiting the optimal correlation with one-dimensional heat dissipation path according to the JESD51-14 standard.

By applying a uniform heating power outlined in Section 3, we can capture the transient temperature response curve. The parameters for the measurement are listed in Table 1.

Table 1. Test parameters

TIM material	No TIM	With TIM (PCM)
Heating Power (W)	80	300
Heating time (s)	300	
Measurement time (s)	600	
Sensing current (mA)	1.0	
Coolant temperature (°C)	25	
Coolant flow rate (L/min)	2.0	

The TIM used in our experiment is a phase change material (PCM). The PCM utilizes a non-Silicone based material, filled with thermally conductive fillers. Through spring loading and pre-heating processes, it can achieve a very low bond line thickness (BLT) of 20 to 30 um. The PCM requires a pre-baking step which is 60 ℃ for 30 min. according to the Technical Data Sheet (TDS) from the supplier. The pre-baking is performed after the assembly of the cooling plate, with temperature regulation maintained by the coolant.

The measurement technique employed is the transient method in accordance with JEDEC51-14, which entails recording the temperature cooling curve immediately following the heating process. By measuring the transient temperature curve under the conditions (with and without TIM), two Z_{th} curves were obtained. Different heating power values were employed to allow the optimal temperature increase for both scenarios, ensuring that it is neither excessively high nor too low. According to the JESD51-14 standard, the θ_{JC} can be evaluated at the separation point of the two Z_{th} curves. Fig. 11 shows an example for extracting the θ_{JC} value from the two Z_{th} curves for the central sensor. The θ_{JC} measured is 4.4 °C/kW, and the θ_{JA} with TIM is 49.4 °C/kW. The low θ_{JA} and θ_{JC} values signify that the designed TTV and TIM are highly efficient in heat dissipation, which is particularly critical for high-power HPC chips.

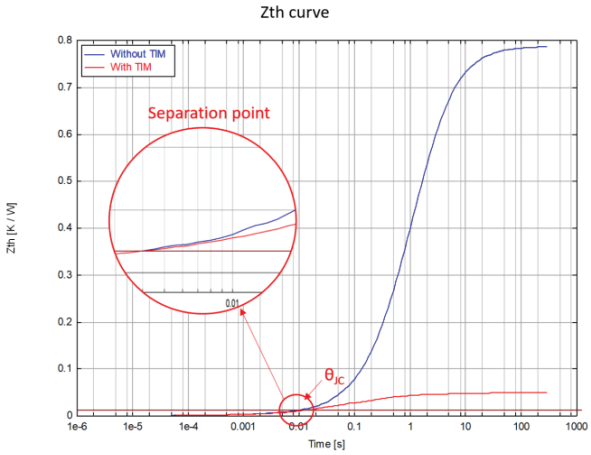

Fig. 11. θ_{JC} value by two Z_{th} curves measured at the central sensor (with and without TIM) using the test setup in Table 1 (heating power with TIM: 300W, without TIM: 80W).

Furthermore, the structure function can be obtained from the transient temperature curve, which allows for a qualitative structural interpretation of the thermal impedance path for the system if assuming that the thermal path consists of a 1-D network as shown in Fig. 12. The structure function features the X-axis representing thermal resistance (R_{th}) and the Y-axis denoting thermal capacity (C_{th}). Through the analysis of this structure function, we gain a profound insight into the thermal performance across various material layers. The structure function indicates that the TIM and the cooling plate may account for the majority of the θ_{JA} of the package.

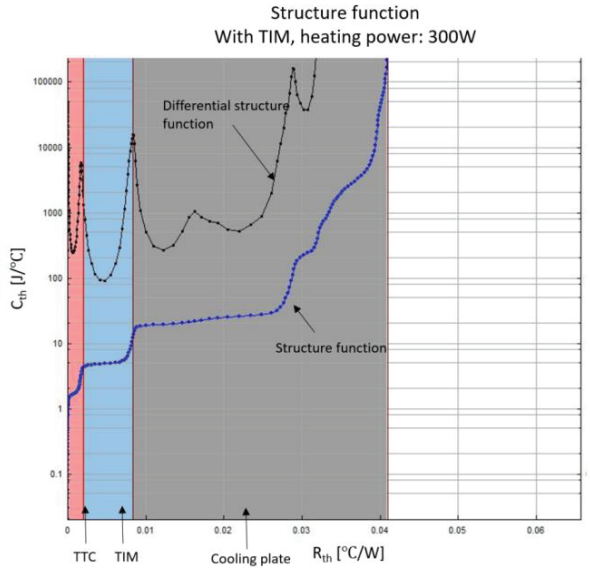

Figure 12: The structure function (at the central sensor) provides information about the structural behavior of the thermal impedance and delineates the different material layers of the package from its curve progression.

4.4 TIM and coolant flow rate characterization

By measuring the T_j and θ_{JA} with various TIMs applied across the entire thermal test chip (TTC) area, we can also characterize the thermal performance of the TIM for the application, which will be published later

The impact of the coolant flow rate is another parameter to study regarding the total θ_{JA} of the package system. An optimal flow rate not only improves effective heat dissipation but also saves energy for the application.

We used the central sensing diode to measure the θ_{JA} of the package under different flow rate conditions with one type of TIM applied. The results are shown in Fig. 13. The trend indicates that the flow rate has a non-negligible influence on the θ_{JA} value.

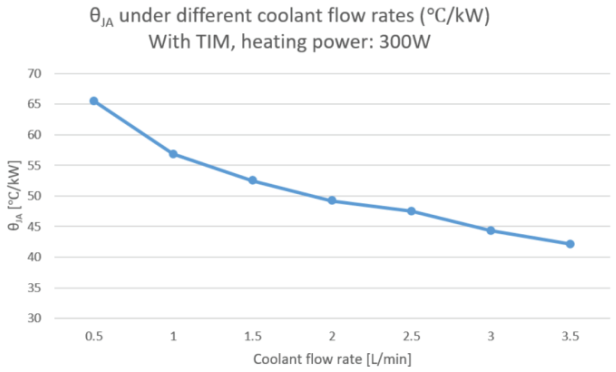

Fig. 13. θ_{JA} under different coolant flow rates using the test setup in Table 1 (at the central sensor).

5. Summary

This study demonstrated the characterization of thermal performance through a TTV design, which is intended to support the advancement of AI/HPC technology with increased complexity and larger die sizes within the chip package. An array of 5 x 5 heating zones is integrated into one TTC, with each TTC containing multiple sensing diodes for in-situ temperature measurement. The TTV, as a crucial tool, offers the flexibility to assess various locations throughout the entire TTC area with uniform or non-uniform power distribution. By connecting all the heating zones in parallel, the TTC can be heated up uniformly through a constant current. Assessing the θ_{JA} and θ_{JC} by analyzing the steady-state or transient temperature profiles provides a thorough understanding of the overall thermal dissipation performance.

Based on the study, we can obtain the following results:

- By applying uniform heating on the primary main TTC, the central sensing diode was chosen to carry out transient characterization in order to determine the structure function.
- The θ_{JA} and θ_{JC} were assessed using the TTV. Structure function can also be derived from the measurements. It is also possible to characterize the effects of various coolant flow rates.
- The TTV design is very suitable for its intended purpose for thermal characterization, specifically in assessing the Tj and Rth distribution of different areas for large body size chips.

These findings highlight the feasibility of the transient thermal characterization by using the TTV design for AI/HPC chip package application. The exceptional utility of the TTV tool will facilitate the progress of package thermal design and characterization, ultimately for developing effective thermal management solutions. Non-uniform heating and characterization of different TIMs will be the subject of further study.

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