THERMAL TEST CHIPS

TTC-1001

(1mm X 1mm Unit Cell)
Wire Bond or Flip Chip

DESCRIPTION

The TTC-1001 thermal test chip is designed to provide a maximum of flexibility for thermal characterization of semiconductor packages. Each Unit Cell can be used individually or in a square or rectangular array. A diode sensor for temperature measurements is in the center of the Unit Cell layout. This diode, when in arrayed cell configuration, can be individually addressed, allowing for temperature contour measurements across an array. The heating resistor in each cell of an array can be powered individually or wired in a series or parallel configuration for operation from a single power supply. In an array configuration, there are several resistor series strings that can be individually powered from separate power supplies or paralleled for operation from a single supply. The multiple cell array design allows for thermal measurements with non-uniform heating across the array.

FEATURES

- **Proven silicon technology: same as the TEA TTC1002 (2.5mm Unit Cell)**
- **Format: bumped/flip chip or wire bond wafers or arrays of Unit Cells**
- **Kelvin connections to heating resistors for improved measurement accuracy**
- **Array form factor: may be arrayed square or rectangular**
- **Array configurations: may be arrayed in up to 20 x 19 Unit Cells**
- **Wire bond: on-chip adjacent cell interconnections of resistors and sensors providing for parallel or series or parallel/series resistor connections with peripheral pad wire bonding**
- **Bumped: all resistors and sensors may be individually connected**
- **One each resistor and sensor per Unit Cell; many resistors and sensors in arrays**
- **Uniform and non-uniform heating and planar temperature contours capable**
- **Suitable for both steady-state and transient thermal measurements**

Contact TEA for:

► **ReDistribution Layer (RDL) options**
► **Bump material composition options, including copper pillars**
► **Backside metal and thinning/polishing options**

SPECIFICATIONS

Electrical - Heating	TTC-1001
# of Resistors	1 **(see Figure 2)**
Resistance Value	10.5 Ω ±10 %
Resistance Variation	±7.5 % (for die from a specific wafer)
Heating Resistor Power Dissipation for $T_J \leq 150^{o}C$	4W (~6.3V @ ~0.63A) max for 1ms 3W (~5.5V @ ~0.55A) max continuous
Connection	Force & Sense wire bond or bump pads
Resistor Coverage	>69% of die area within wire bond or bump pads

over, please

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Electrical - Sensing	**TTC-1001**
# of Diodes	1 center
Nominal V_F	0.74 V @ I_F = 1 mA each diode
Nominal BV_R	7 V @ I_R = 10 µA each diode
Addressing	Row and Column wire bond or bump pads
Physical	
Wafer Size	152 mm (6 inch) Diameter Nominal
Unit Cell Size	1.00 X 1.00 mm **(0.0394 X 0.0394 inch)**
Die Layout	See Figure 1
Array Capability	See Figure 3
Wafer Thickness	625µm **(0.025 inch)** Nominal **(thinning optional)**
Scribe Line Width Between Cells	76µm
Wafer Backside Finish	Ground, un-polished **(polishing optional)**
Wafer Yield	Greater than 80%
Approximate Unit Cells/Wafer	>8,000
Wire Bond Pad Size	100µm **(0.00394 inch)** diameter
Wire Bond Pad Material	Al-Si**(1.0%)**-Cu**(0.5%)**
Bump Materials available	• Lead-Free • Low-Lead • SAC305 • High-Lead
Bump Size	~90µm diameter, ~85µm height

Figure 1 Unit Cell Layout

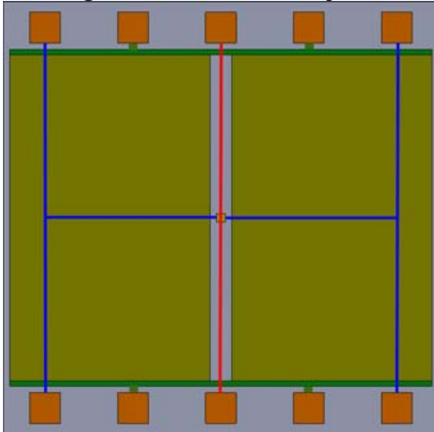


Figure 2 Unit Cell Schematic Representation

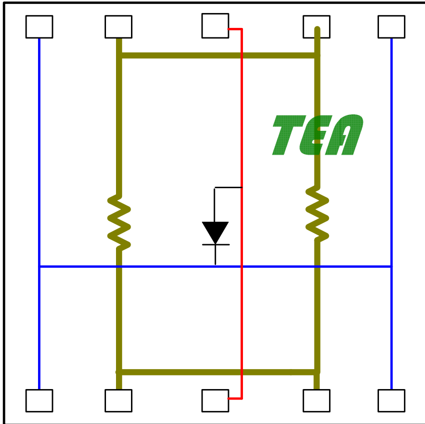
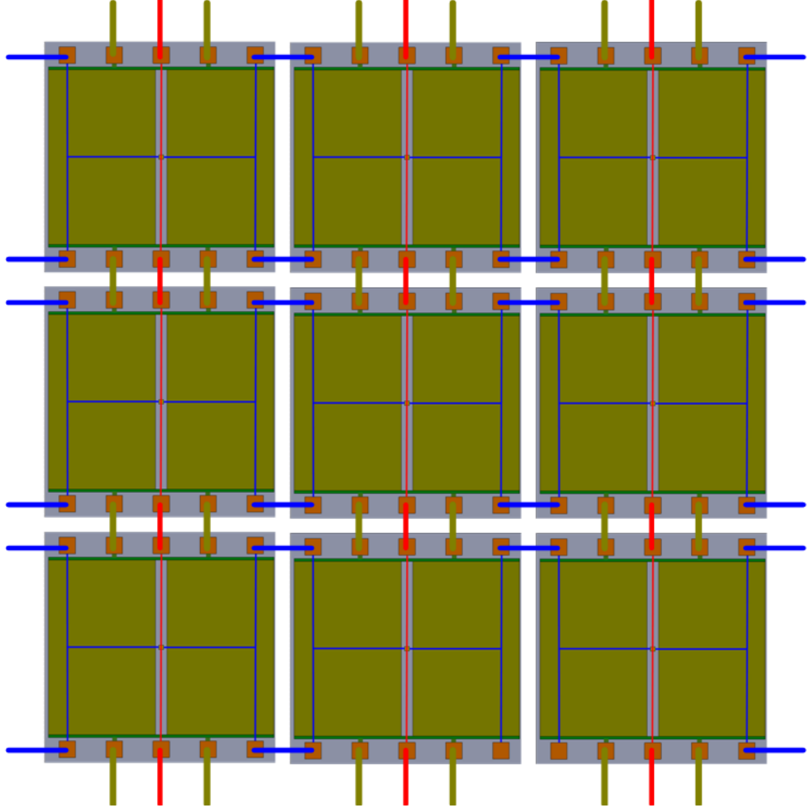


Figure 3 Typical Array Layout (Shown as 3 X 3 array)



Cell-to-Cell Interconnects ▬ Diode Anode ▬ Diode Cathode ▬ Resistor

Included in Wire Bond version; must be implemented in Bump version on package substrate or on pcb

For assistance in electrical connection of Unit Cells in an array configuration, please contact TEA with your specific array requirements.