THERMAL TEST BOARDS

TTB-1000 Series

DESCRIPTION

The TTB-1000 Series of thermal test boards conform to the newly developed JEDEC standards defined by the JESD51 series of documents. Also included in the TTB-1000 Series are boards conforming to standards currently under development by the EIA/JEDEC JC15.1 Subcommittee on Thermal Characterization of Electronic Component Packages.

These boards provide a well defined mounting environment for the thermal characterization and comparison of packages containing either thermal test or application die. Each package lead land is fanned out with an eyelet termination to allow for hand-wired connection to the board edge contacts. The board material will withstand temperatures to 125 °C, allowing the board/package combination to be used for temperature calibration as well as thermal measurements.

The Series consist of three separate groups of boards. The first group is for smaller component packages that fit on a 76.2 X 114.3 mm (3” X 4.5”) printed circuit board. These boards are offered in both low thermal conductivity (low K_{eff}) and high thermal conductivity (high K_{eff}) versions. The former is a board with minimal copper traces on both sides, referred to as a 2s board. The latter is a board with two internal copper planes as well as the surface traces, referred to as a 2s2p board. The second group of boards. for larger component packages having a body dimension ≥27 mm, has outline dimensions of 101.6 X 114.3 mm (4” X 4.5”), and is also available in low and high K_{eff} versions. The third group is for special packages, such as Ball Grid Array (BGA) styles, that have special requirements and/or non-standard pinouts. Included in this group are custom boards intended for newly developed packages for which no current standards or standards activity exists; TEA offers these boards designed to conform with the general intent of the JEDEC standards.

FEATURES

- **Conforms to industry standard specifications**
- **Available in both Low and High K_{eff} versions**
- **Accommodates most standard IC package styles**
- **Board edge connector provides for Kelvin connection to improve accuracy**
- **Multiple sizes to accommodate a wide range of package characterization requirements**
- **Package lead-to-edge connector user-wired for maximum flexibility**
- **Custom versions in general conformance to standards available for special requirements**

over, please

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SPECIFICATIONS

Package Style	Body Dimension	# of Leads (see Note 1)	Lead Pitch	Low K_{eff}	High K_{eff}
*Universal Design**					
DIP	0.300″ wide	8 to 22	0.10″	TTB-1101	TTB-1201
DIP	0.600″ wide	22-34	0.10″	TTB-1102	TTB-1202
SOIC (gull wing)	0.150″ wide	8 to 28	0.050″	TTB-1103	TTB-1203
SOIC (j-lead)	0.150″ wide	8 to 28	0.050″	TTB-1104	TTB-1204
SOIC (gull wing)	0.208″ wide	8 to 28	0.050″	TTB-1105	TTB-1205
SOIC (j-lead)	0.208″ wide	8 to 28	0.050″	TTB-1106	TTB-1206
SOIC (gull wing)	0.300″ wide	8 to 32	0.050″	TTB-1107	TTB-1207
SOIC (j-lead)	0.300″ wide	8 to 32	0.050″	TTB-1108	TTB-1208
SOIC (gull wing)	0.400″ wide	8 to 32	0.050″	TTB-1109	TTB-1209
SOIC (j-lead)	0.400″ wide	8 to 32	0.050″	TTB-1110	TTB-1210
SOT-23	0.051″ wide	3 to 6	0.0375"	TTB-1111	TTB-1211
TO-252	6.58 mm	3	2.285 mm	TTB-1112	TTB-1212
TO-263	0.400″ wide	3	0.100"	TTB-1113	TTB-1213
TSOP II	0.400″ wide	66	16.5 mm	TTB-1120	TTB-1220
TSOP II	0.400″ wide	54	20.3 mm	TTB-1121	TTB-1221
QFP	10 X 10 mm	44	0.5 mm	TTB-1303	TTB-1403
QFP	12 X 12 mm	80, 100	0.5 mm	TTB-1304	TTB-1404
QFP	14 X 14 mm	120	0.5 mm	TTB-1305	TTB-1405
QFP	28 X 28 mm	144 to 240	0.5 mm	TTB-1301	TTB-1401
QFP	28 X 28 mm	256	0.4 mm	TTB-1302	TTB-1402
*Dedicated Design***					
BGA	27 X 27 mm	225	1.50 mm	See Note 2	See Note 2
BGA	35 X 35 mm	352	1.27 mm	See Note 2	See Note 2
BGA	35 X 35 mm	480	1.27 mm	See Note 2	See Note 2
BGA	40 X 40 mm	256	1.00 mm	See Note 2	See Note 2
BGA	40 X 40 mm	480	1.00 mm	See Note 2	See Note 2
BGA	40 X 40 mm	758	1.00 mm	See Note 2	See Note 2
BGA	15 X 15 mm	256	0.80 mm	See Note 2	See Note 2

* ***Universal Designs -*** Contact traces brought out to solder eyelets for wiring the packages in any configuration.

** ***Dedicated Designs -*** Contact traces are custom designed to match package's specific pin-out thermal ball requirements. Packages shown represent those already designed by *TEA*.

Note 1: **Lead number range indicates a nested board design**
Note 2: **Custom design – contact *TEA* for information**

Please contact *TEA* for information on package styles or board types not shown above. Boards conforming to the SEMI standards and for custom packages (such as for optical integrated circuits and RF/Microwave devices) are also available.

Specifications subject to change without notice.
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