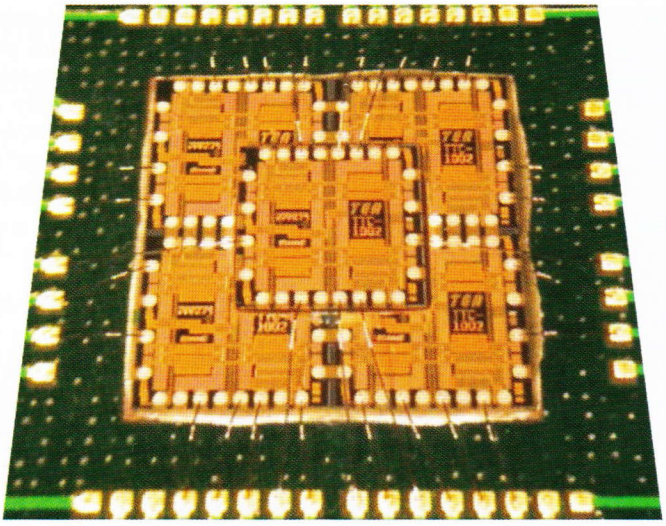
Thermal design validation techniques

Modern thermal test chips can provide both the heat and means for temperature measurement

Joe Fjelstad



Thermal test chips aid in proofing new package designs employing stacked chip assemblies such as is shown above. Image courtesy of Thermal Engineering Associates, Inc.

Heat is the bane of semiconductor devices, and yet it is a natural byproduct of their operation. There is in fact an inverse relationship between product reliability and the range and number of number thermal excursions experienced by a semiconductor device; thus knowing what kind of thermal challenge is presented by a particular design is key to addressing and solving the problem in an intelligent and proactive way. While finite element modeling of an electronic product is a very useful and important tool for identifying potential problem areas in an IC package structure, there is nothing like empirical experimentation and results to provide the kind of data that the practical line engineer likes to see and work with before sending the product out into the world. While the challenge of prediction and preemption of problems has been a part of IC packaging design efforts for many years, the current trend in stacking chips within packages raises the level of challenge to new heights (no pun intended).

One response to that challenge has been the development of thermal test chips or TTCs. Fundamentally these test chips are semiconductor devices that contain at least one heat-generating element and at least one temperature-sensing element to measure and control the output of the heat-generating element. In practice, the heat-generating element can be as simple as a resistor or as complex as a large area bi-polar junction transistor (BJT) or metal oxide semiconductor field effect transistor (MOSFET). In most test chip designs, resistors are often chosen because of the simplicity of design and use; however designs employing transistors are better suited for designs where very high total heat generation and heat flux density generation are desired. However, to use the transistor's inherent temperature-sensing capability, fast switching at high power levels is required. With respect to TTC temperature sensing, the sensing element can also be a resistor, but one with a well-defined resistance-temperature relationship such as a thermistor or resistive temperature dependent device (RTD). The other choice for sensing is a semiconductor junction, which has its own specific and well-defined forward voltage (VF) – junction temperature (TJ) relationship.

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Traditional applications for thermal test chips have included 1) Evaluation of new or current IC package ability to meet thermal requirements. 2) Thermal simulation and verification of package capability. 3) Evaluating package mechanical response to stress generated by internal thermal testing loads. 4) Mapping of thermal effects, both local and global, and 5) both board and system level thermal simulation.

From the user's perspective there are a number of key requirements demanded of thermal test chips to assure they will fulfill the needs of the applications recounted above. These requirements include the following: First the device should provide the largest possible heating surface area relative to chip size while providing uniform temperature profile across the area. The device should preferably have a low temperature coefficient for the heating source and should ideally have a temperature sensor in the center of the chip as well as other sensors across the chip surface, allowing the user to establish a temperature profile. The temperature sensors should be simple to use and should preferably employ Kelvin connections (i.e., 4-wire connections) to assure measurement accuracy. Finally, the thermal test chip should be a size that closely approximates the size of the chip which is being simulated.

One such chip is presently available from Thermal Engineering Associates, Inc. (www.thermengr.com) in Santa Clara, CA. The new chip was engineered to comply with EIA/JESD51-4 "Thermal Test Chip Guidelines." According to the developer, their test chips are flexible enough to meet virtually all of the requirements for general purpose semiconductor thermal testing applications. The test chip provided by the developer is based upon a novel unit cell design which is 2.5 mm on a side and

which is repeated to form up to a 40x40 matrix. This allows the user to activate one cell individually or combine and activate as many cells as needed up to the limits of the matrix. Regardless of the number of cells chosen, periphery connections provide access for all heating and Kelvin-enabled measurement need. In use, strategically

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placed diode sensors enable temperature measurements in the center, center periphery and opposite diagonals, regardless of the size or configuration of the cell array, and two individual metal film heating elements, which may be connected in series or in parallel, cover 87% of the die surface to provide uniform heating to each half of the cell, as needed. Moreover, a 4x4 unit cell array can handle up to 192 W, thus providing a power density of 183 W/cm^2, which is beyond current generation need for most electronics but which also opens the door to the test chip's application in other areas and types of product development where thermal conditions and/or control are a driving concern.

While thermal test chips have been widely used to help mitigate or eliminate electronics heat dissipation problems from package to system level, provide thermal characterization, facilitate package assembly process optimization and improve heat sink thermal solution evaluation, they have also proved of value when semiconductor manufacturers do final test on packaged semiconductor devices. As mentioned earlier, this is increasingly important with new designs where chips are stacked on top of each other inside the package. The potential to thermally exercise and measure temperatures on chips that reside at the center of a stack will likely be increasingly important in the future.

In use, package development engineers commonly desire to make parametric and functional measurements over an extended temperature range such as 0°C to +70°C for consumer electronics or -25°C to +85°C for more demanding commercial products. These temperature ranges refer to the junction temperature. Unfortunately most of the time the manufacturers have no way to actually make this measurement. Thus by putting a thermal test chip into the same package as they are trying to test, development engineers have a way to monitor the junction temperature after the device has been subjected to preconditioning and has been inserted into the test site. This is an important consideration because transistor leakage tends to double with every 10°C increase in junction temperature. The implications can be significant. For example, if the manufacturer thinks the junction temperature is at a certain point but the actual temperature is higher, there could be failed devices much earlier in the life of the device than anticipated or desired. Moreover, most semiconductor parametric and functional characteristics are temperature sensitive, and not knowing the actual junction temperature during the final test process can be costly either by yield reduction through infant mortality or more onerously by early field

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Another use for this technology is in the realm of SMT assembly process development. Surface mount process engineers are familiar with the current slate of options and tools, which are comprised of some tried and true methods; however the advent of lead-free soldering has taken the industry to the limits, and the IC packages and PCB are more vulnerable than at any time in the past due to the high temperatures that are required process lead-free solder. Thus it appears that these versatile devices should capable of serving as an alternative to current temperature profiling tools, providing more detailed information to the user as to what is actually happening in the package during reflow.

In summary, given the growing list of challenges facing the electronics assembly industry thermal test chips appear well-positioned to help engineers identify and remedy potential thermal problems before they hit the field rather than after. The ability to accurately measure and track temperature excursions inside the chip package by means of thermal test chips is a valuable tool in accomplishing that objective.

1. http://www.jedec.org/download/search/jesd51-4.pdf

Verdant Electronics founder and president Joseph (Joe) Fjelstad has more than 40 years of international experience in electronic interconnection and packaging technology in a variety of capacities from chemist to process engineer and from international consultant to CEO. Mr. Fjelstad is also a well known author writing on the subject of electronic interconnection technologies. Prior to founding Verdant, Mr. Fjelstad co-founded SiliconPipe a leader in the development of high speed interconnection technologies. He was also formerly with Tessera Technologies, a global leader in chip-scale packaging, where he was appointed to the first corporate fellowship for his innovations. He has 150 US patents to his credit.