Thermal Effect of Die Bond Voids

Analysis of the effect of die bond voids on thermal performance of ceramic, metal and plastic packages.

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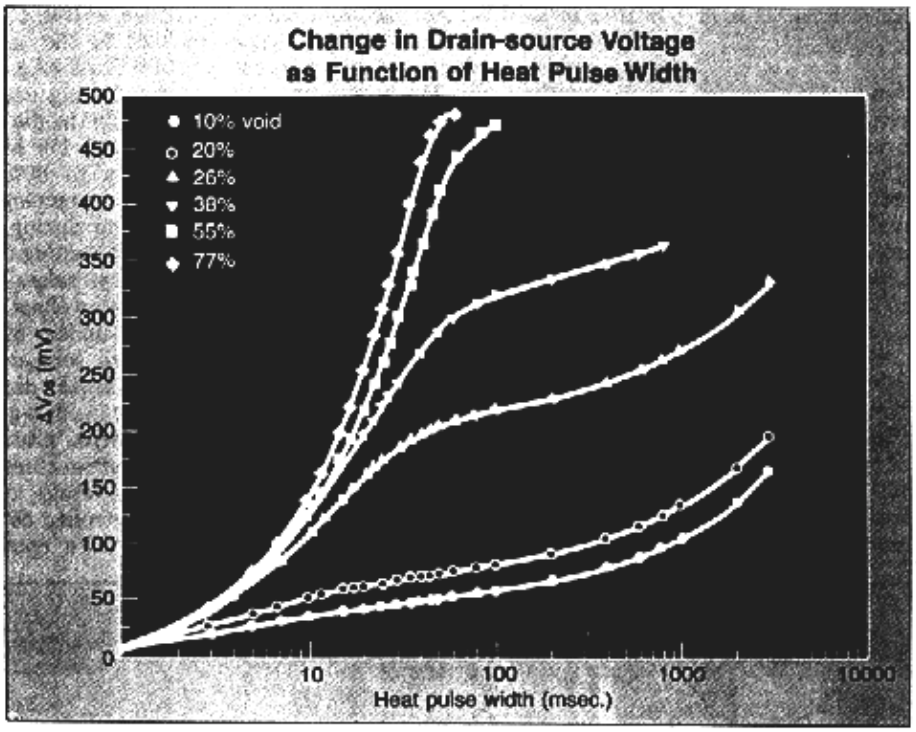

1. Change in drain-source voltage (ΔV_{DS}) as a function of heat pulse width for TO-3 metal packages with soft solder die attach and varying degrees of voiding (10%-77%).

In the operation of many semiconductor devices, the effective dissipation of internally generated thermal energy is critical to both device performance and the component's reliability. A device's useful lifetime is an exponential function of junction temperature, decreasing by approximately a factor of two for every 10°C increase in temperature[1]. In the last few years, however, increased focus on quality and reliability has rejuvenated interest in minimizing the junction temperature to slow the metallurgical/materials interactions commonly causing failure[2]. This concern is compounded in new bipolar IC and discrete power devices with higher device powers and/or higher power densities. In addition, many system houses, while deeply concerned with system reliability, are employing higher ambient temperatures and greater restrictions on usable cooling techniques. The emphasis on increasing device power and power densities, higher ambient temperatures and improved reliability, leaves no alternative but to reduce thermal resistance by using improved thermal management techniques.

The scope of work presented in this article was to examine the effect of both small, randomly distributed voids and larger, contiguous voids in the die bond on the thermal performance of three package constructions: the TO-3 metal package, the 24-lead CERDIP and the 40-lead plastic DIP (p-DIP). These adequately represent the gamut of packages commonly used to house power dissipating devices. Two techniques employed for measuring the thermal performance of the packages are the transient parametric method[3] and the steady state infrared (IR) scanning technique. In addition, finite difference modeling simulations are compared to the experimental measurements.

Thermal measurement technique

Two techniques were used to quantitatively evaluate the thermal effects due to voids in the die bond. For the thermal transient test, a Sage tester (Model DAE 230) was used. Heat pulses of fixed amplitude (50W for metal packages and 35W for CERDIP and p-DIP's) but durations ranging from 1 ms to 1 s were applied to the device. The change in the drain-source voltage (V_{DS} in mV) before and after applying the heat pulse was measured. Such data are plotted as ΔV_{DS} vs. heat pulse width in Fig. 1 for TO-3 packages with varying degrees of voiding (10-77%) and show that a 20 ms duration heat pulse will discern the nature of the die bond interface. Later, the data base was constructed by collecting ΔV_{DS} for a 20 ms wide heat pulse.

The second technique, a steady state scanning method, employed an RM2A IR microscope. The packages were

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mounted in good thermal contact on a water cooled heat sink. The device and header surfaces were scanned with the microscope and both the hottest temperature and the temperature gradients recorded. For detailed temperature distributions on the die and header surfaces, the microscope's spatial resolution of 0.1 mm and temperature resolution better than 0.5°C served quite adequately. The package's case temperature was measured with a fine wire thermocouple. The hottest temperature on the device was used to determine the thermal resistances such as Θ_{JH} and Θ_{JC}.

Device characteristics

A uniform heat source is preferable to represent the power dissipating chip in evaluating thermal effects of voids. This eliminates any artifacts in the data due to temperature nonuniformities in the heat source. An actual device was chosen over a deposited thin film heat source because of its easy availability and the applicability of the thermal transient technique. A TMOS power transistor was selected because of a nearly uniform heat source pattern over the entire device surface. Figure 2a is a top view schematic of the TMOS power device and each line element corresponds to a current carrying channel, nearly 45 μm wide and spaced 45 μm apart. Each channel is a line element heat source and the heat source is located close to the top surface of the chip. Figure 2b is an IR image of the packaged TMOS device (TO-3) mounted on a water cooled copper heatsink and dissipating about 78 W. The die bond is essentially voidfree and the IR image verifies the near uniformity of the heat source.

Package construction

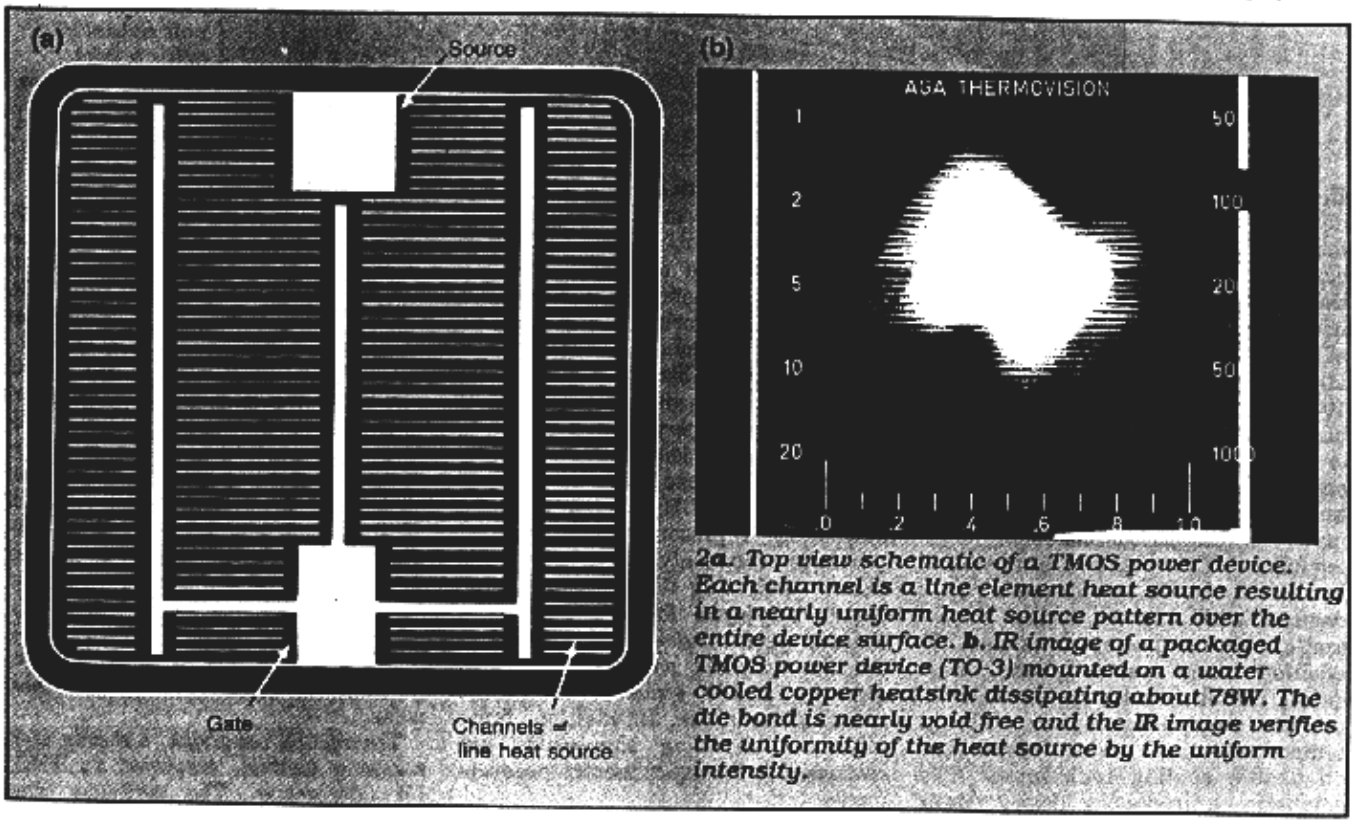
The TO-3 steel package is sketched in Fig. 3a. The OFHC copper header is brazed to a 1020 steel case and plated with electroless nickel. T_J, T_H and T_C are the junction, header and case temperatures, respectively. The heat generated at the junction travels through the silicon bulk, the solder bond and around the voids, and through the copper header to the steel case. The solder is the poorest thermally conductive component in the package. The TO-3 aluminum package (Fig. 3b) utilizes the electroless nickel plating on a 5052 aluminum header. The thermal performance of this construction is poorer than the TO-3 steel package, but allowed nondestructive void characterization with epoxy die attach.

Figure 3c illustrates the 24-lead CERDIP package construction. In this case thermal dissipation is primarily undirectional through the solder bond into the Al_2O_3 substrate. This is in contrast to the 40-lead p-DIP shown in Fig. 3d where conductive heat flow is divided between the epoxy die bond to the copper alloy leadframe versus directly into the overmold epoxy in contact with the chip.

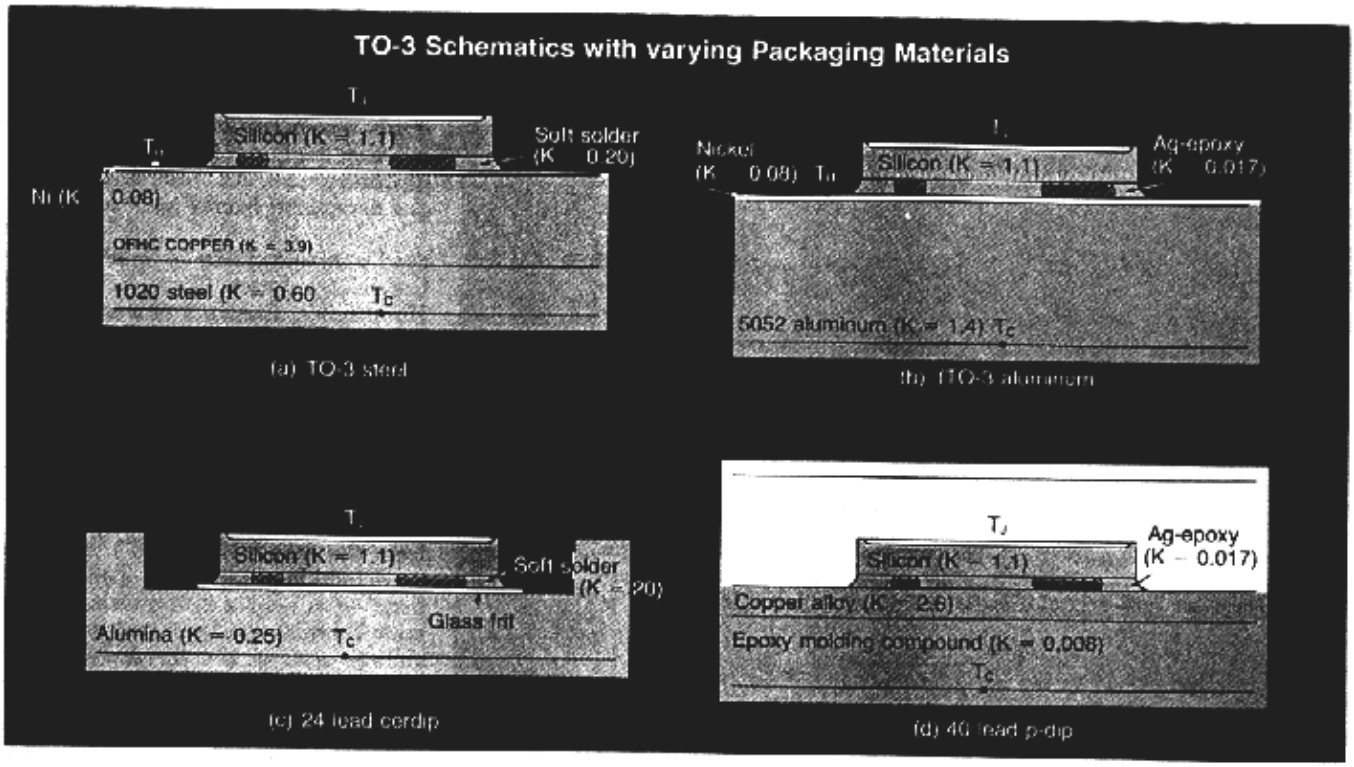
Solders/adhesives/die bonding

Soft solders were used for die attach in the TO-3 steel and 24-lead CERDIP packages and silver filled organic epoxies in the 40-lead p-DIP and TO-3 aluminum packages. To effectively produce a low concentration of voids (5-30%) in the soft solder die bonds, 92.5Pb-5In-2.5Ag solder preforms were used following assembly procedures in which only the die bonding temperature was varied. For higher void concentrations (up to 80%), 75Pb-25In solder cream was employed in which solvent outgassing during die attach produces excessive voiding unless special precautions are taken. The TO-3 solder assembly involves die bonding in a belt furnace under hydrogen atmosphere with peak temperatures of 370-470°C. The CERDIP die bonding was done manually inside a glove box continuously purged with nitrogen and the heater block temperature was kept at 400-420°C. Average die bond thicknesses were controlled between 38 and 58 μm.

Conductive epoxy was employed in



2a. Top view schematic of a TMOS power device. Each channel is a line element heat source resulting in a nearly uniform heat source pattern over the entire device surface. b. IR image of a packaged TMOS power device (TO-3) mounted on a water cooled copper heatsink dissipating about 78W. The die bond is nearly void free and the IR image verifies the uniformity of the heat source by the uniform intensity.



3a. Schematic showing construction of TO-3 steel package with soft solder die attach. Shaded areas in solder represent voids and K values are material thermal conductivities in Watts/cm-°C. Measuring positions for the junction, header and case temperatures are labeled.
b. Schematic illustrating construction of TO-3 aluminum package with silver filled epoxy die attach. K values are material thermal conductivities in Watts/cm-°C.
c. Schematic showing construction of 24 lead CERDIP with soft solder die attach. K values are material thermal conductivities in Watts/cm-°C.
d. Schematic illustrating construction of 40 lead p-DIP with silver filled epoxy die attach. K values are material thermal conductivities in Watts/cm-°C.

assembling both 40 pin p-DIP's and a group of TO-3 aluminum packages. Average bond line thicknesses were controlled between 25 and 55 μm with epoxy curing conditions being 150°C for 15 min. in air. Voiding was controlled by painting the adhesive where desired producing contiguous voids. Peripheral voiding characterized smaller void concentrations while large central voids were typical of severely voided samples.

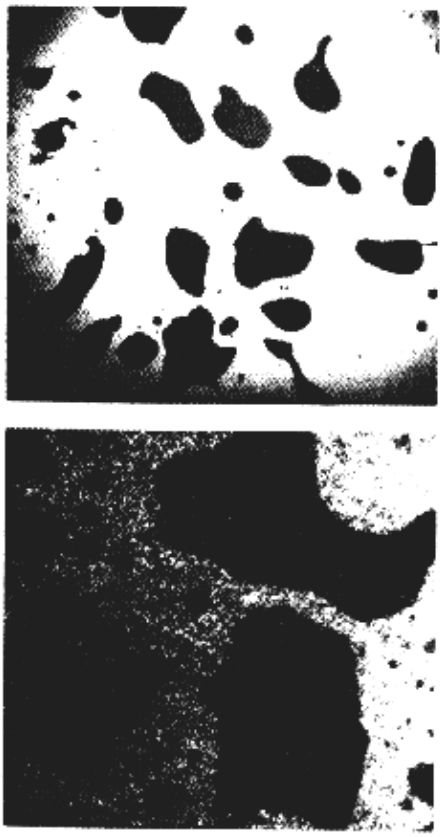
Void concentration measurement

The void area in the die bond was measured from an X-ray photograph of the assembled device. In the case of TO-3 and CERDIP packages with soft solder attach, the area occupied by voids was measured with the help of a 10 × 10 square grid pattern placed on the X-ray photograph. The voided regions in the adhesive die bonded samples were measured by projecting the X-ray slide on a 15 × 15 square grid pattern and counting the fraction of intersections in the void area. Good agreement was obtained between the two slightly differing techniques.

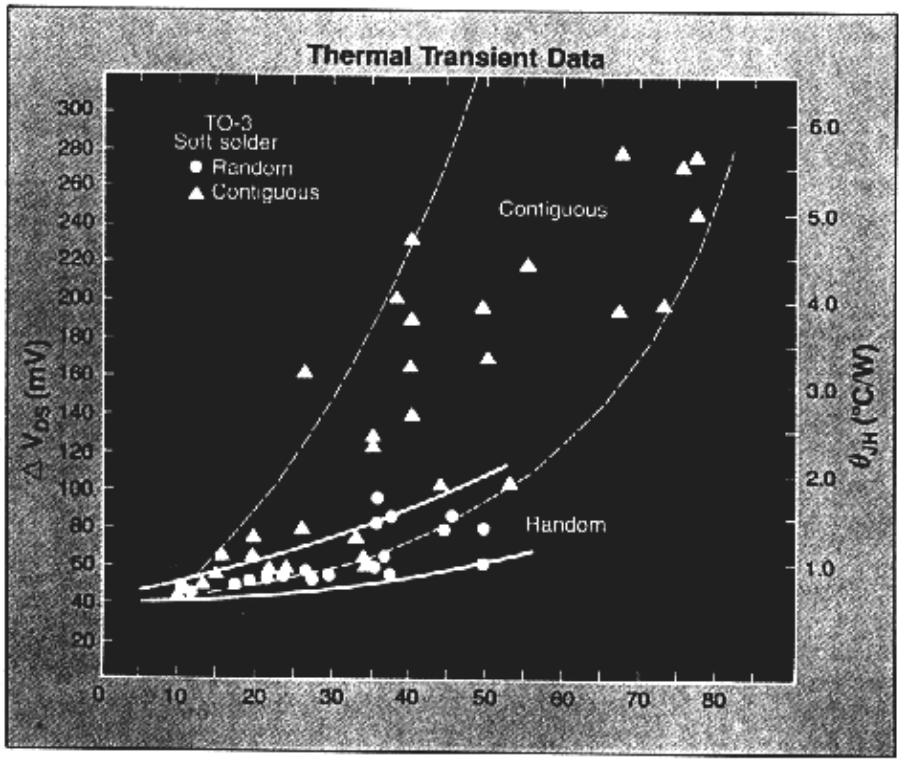
Besides determining the percent voids in the die bond, a qualitative assessment of the character of the voiding was made for the soft solder bonds. Bonds were placed in two categories, random and contiguous. Randomly voided bonds are characterized by a large number of small voids, somewhat randomly dispersed throughout the bond area. In contrast, some bonds had a smaller number of large contiguous voids. Figure 4 shows examples of both random and contiguous voided die bonds.

Experimental results

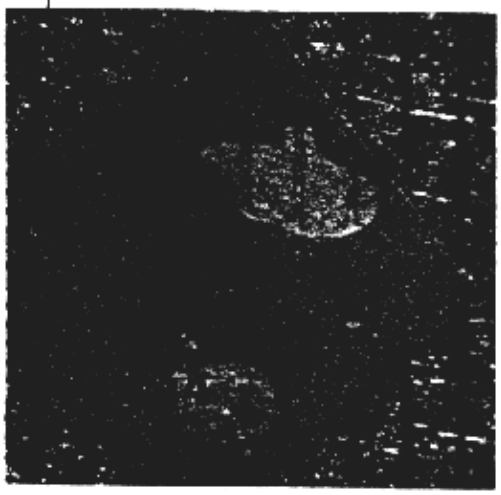
The results section is divided by package type, starting with the best performing package, the TO-3 metal package, and ending with the poorest

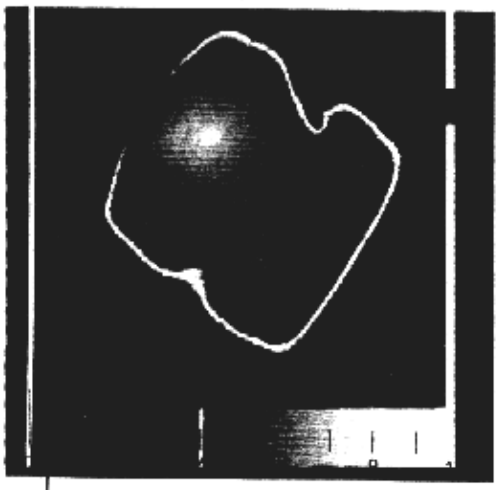


4a. X-ray micrograph showing an example of random die bond voiding. b. X-ray micrograph showing an example of large contiguous voids in the die bond.



5. Thermal transient data (ΔV_{DS} for a 20 msec wide heat pulse) for TO-3 metal packages with soft solder die attach versus percent voids. Voids are categorized as random and contiguous. Junction to header thermal resistances (O_{JH}) are extracted from Fig. 7 and 8.





6a. View of voids after etching off silicon chip. b. IR image of the device in Fig. 6a under steady state power dissipation. Higher intensity represents warmer regions of the chip and corresponds to voided regions in the die bond. The inner isotherm is 7°C warmer than the outer isotherm.

performing package, the 40 lead p-DIP. Discussion centers on the die bond contribution to the thermal resistance and the effect of voiding on this contribution.

Steel TO-3/soft solder

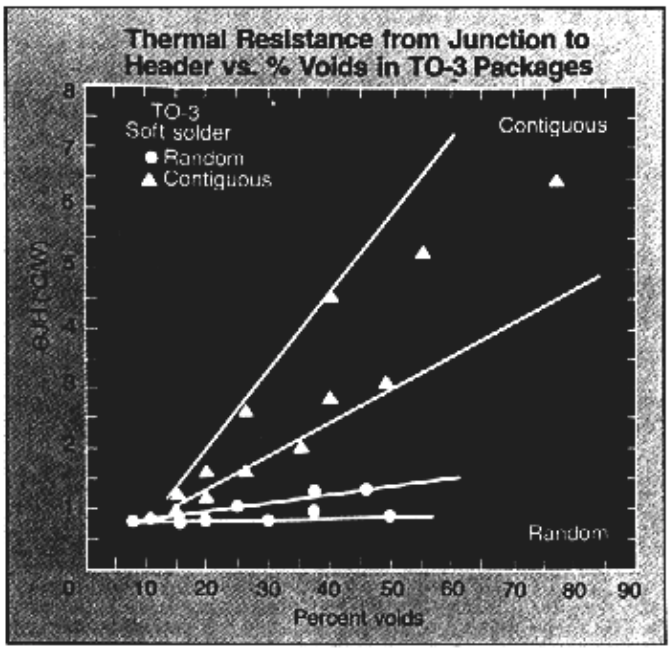
Thermal transient data are plotted in Figure 5 as ΔV_{DS} (for a 20 ms wide heat pulse) versus percent voids in the die bond. The data separate into two bands with some overlap. The lower and upper bands correspond to random and contiguous voids, respectively. There is excellent correspondence between actual voids in the die bond and hot regions in the powered chip. Figure 6a is a view of the die bond after the silicon chip is etched off showing the voided region. Figure 6b is an image of the die obtained with an imaging infrared microscope. The warmer regions of the chip show up in higher intensity and correspond to the voided region in the die bond. A 7°C temperature gradient exists between the two superimposed isotherms. Such a good correspondence is found in most instances between X-ray, etching and IR imaging. Figure 7 is a plot of Θ_{JH} versus percent voids for selected samples from Figure 5. As with the thermal transient data, the steady state thermal resistance separates into two bands, the upper band for contiguous voids and the lower band for random voids.

Several observations can be made from the data in Figure 5-7. First, as expected, increasing the percent die bond voids results in increasing steady state thermal resistance and increasing voltage shift in the thermal transient test. The rate of change is small between 0 and 25% voids, while accelerating when above 30% contiguous voids. The larger contiguous voids give a higher resistance to heat flow than the same area percentage of smaller random voids, with the scatter in the data much larger for contiguous voids. A good correlation exists between the transient and steady state data in Figure 8 where O_{JH} is plotted against ΔV_{DS}. Data from both the random and contiguous categories fall reasonably well on the same straight line. One utility of this plot is that a value of Θ_{JH} can be obtained from a knowledge of ΔV_{DS} (a value that is quite easy to determine). Such values of Θ_{JH} are obtained from this plot and labeled on the right hand margin of Figure 5.

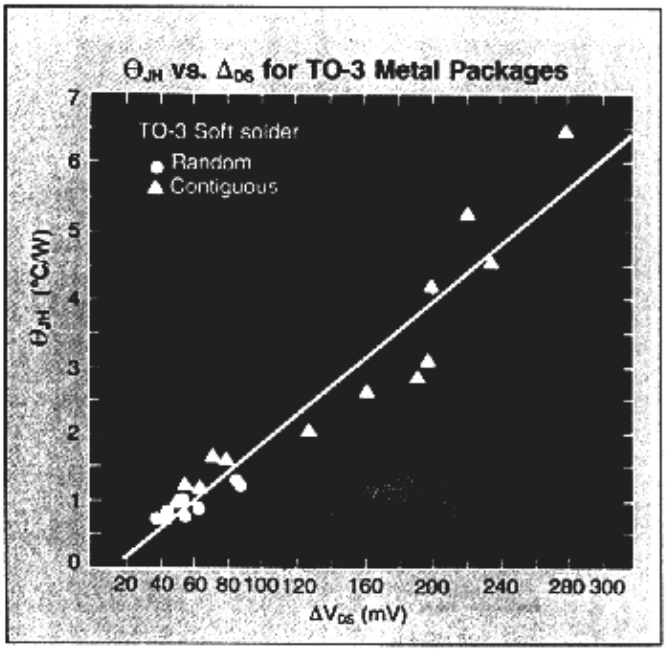
Discussion

It is easy to visualize that increasing percent voids will result in increasing thermal resistance due to decreased area for heat transport. However, explaining the rate of increase with increasing voiding is not so easy. For example, from the data in Figure 7, as the void fraction increases from 10 to 50%, Θ_{JH} increases by nearly 50% and 500% for the random and contiguous cases, respectively. Thus, for a fixed percent voids, the effect of the void size, shape and distribution on resistance to heat flow can be dramatic.

To add additional understanding concerning the effect of void size and shape, computer modeling was performed using a finite difference technique[4]. The TMOS transistor (with a



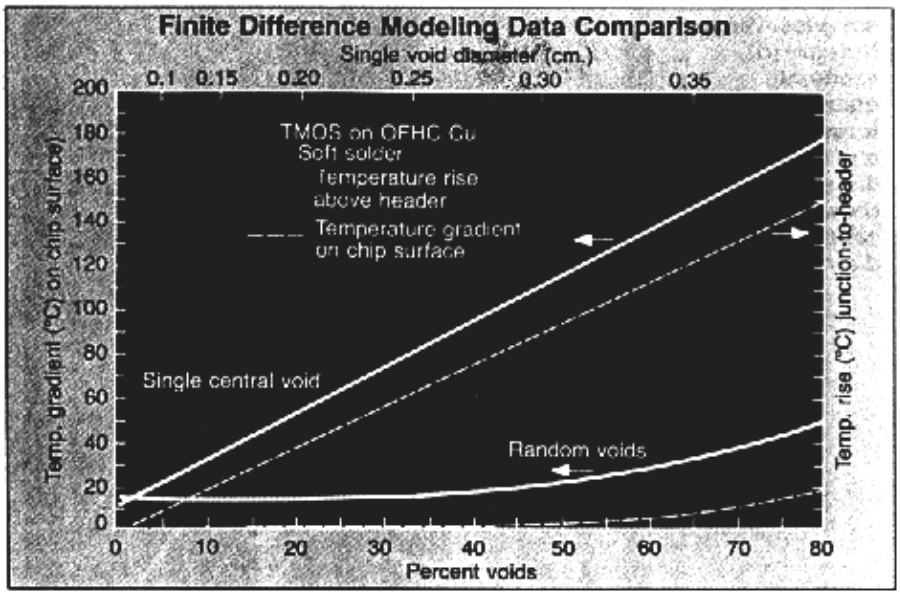
7. Thermal resistance from junction to header (Θ_{JH}) versus percent voids in TO-3 packages. Junction and header temperatures were obtained under steady state power dissipation with an IR microscope.



8. Θ_{JH} versus Δ_{DS} for TO-3 metal packages correlating the steady state and transient thermal measurements.

uniform heat source) was attached on a OFHC copper header with soft solder and powered to 50 W while mounted on a cold plate maintained at 25°C. Models were run with one centrally located void, ranging in diameter from 0 to 0.375 cm. Figure 9 shows both the temperature rise of the junction above the header and the temperature gradient across the chip surface (basically across the void). For a single void diameter above 0.125 cm, the void contribution to the peak thermal rise from junction to header exceeds the normal package contribution. This is because the temperature gradient across the chip surface becomes the major contributor to the total rise in junction temperature.

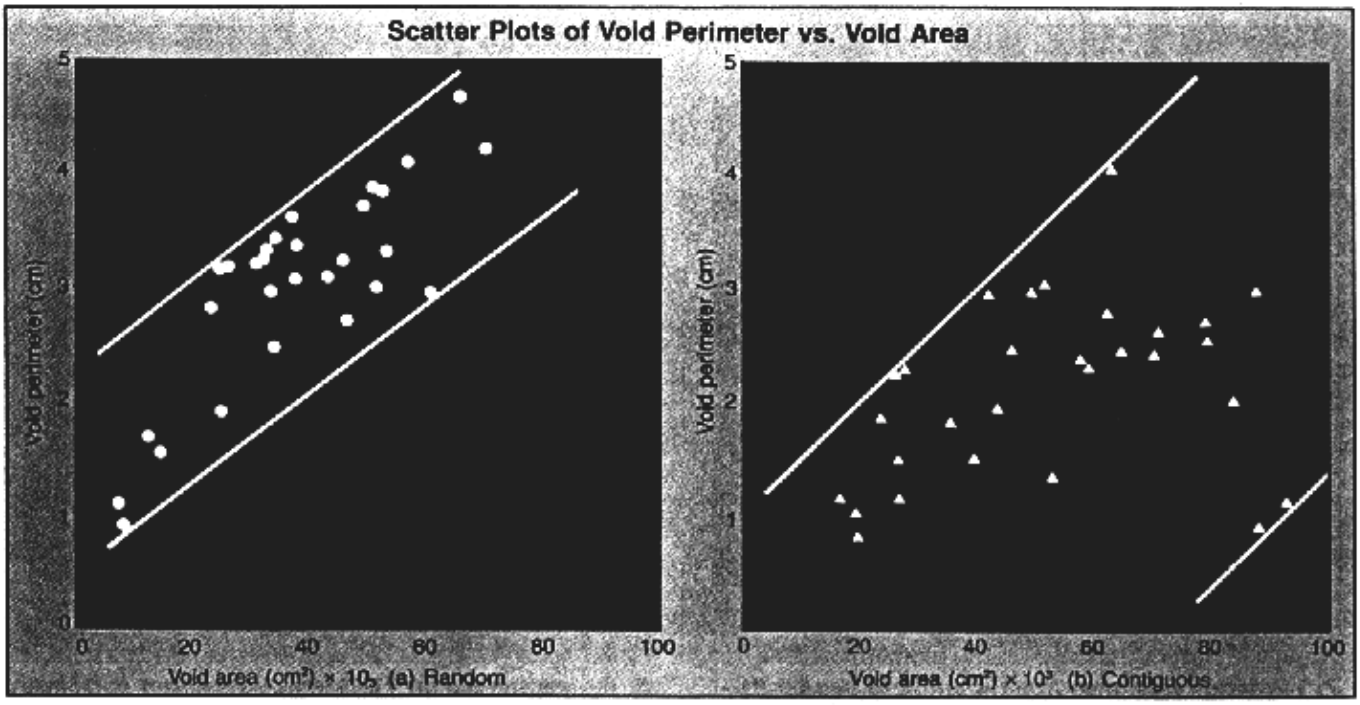
This is quite different from results for the random voiding case with many small voids dispersed uniformly throughout the die bond (lower curves in Fig. 9). Here the effect of voiding on the peak temperature rise from the junction to header (or equivalently Θ_{JH}) is much smaller than for the large single void case. Therefore, it is clear that not only is the percentage of voids important, but so is the void size, shape and distribution in the die bond. The two limiting cases in Figure 9 are bounding cases for real-life applications, with actual packages expected to lie between the curves. Actual temperature gradient and temperature rise data



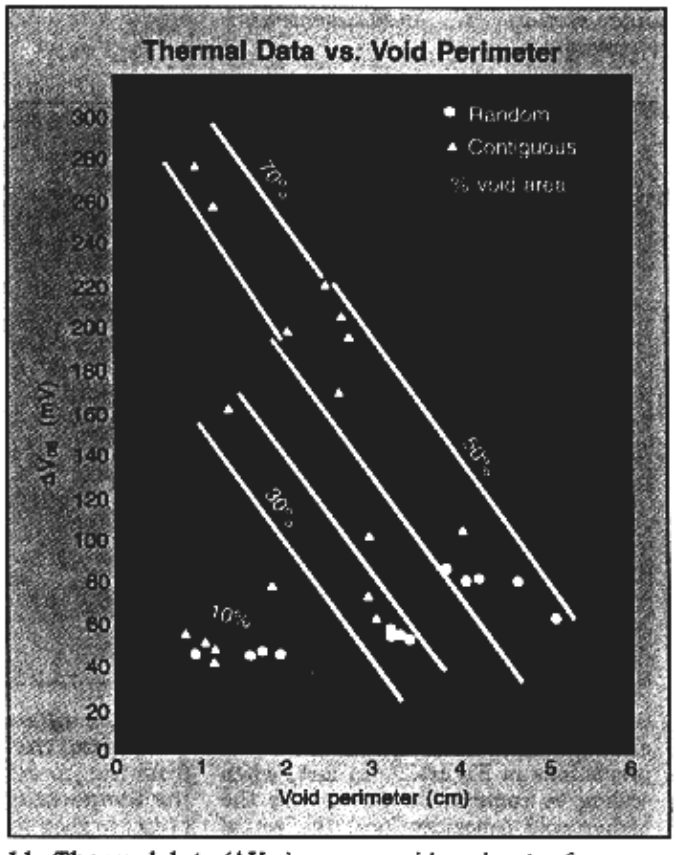
taken with the scanning IR microscope on numerous TO-3 samples confirm the predictions in Figure 9. In fact, when scaling to comparable powers for the higher void concentrations, the actual temperature gradients were often somewhat higher than those predicted in Figure 9.

It is readily shown mathematically that heat flow from a heat source of fixed area will be more effective, the larger its bounding perimeter. The thermal gradient on the chip surface

9. Finite difference modeling data comparing the temperature rise from the junction to header and the temperature gradient over the chip surface for the cases of a single contiguous void versus many small uniformly distributed voids in the die bond.



10. Scatter plots of void perimeter versus void area for TO-3 samples. Voids that are (a) randomly distributed have larger per- imeter and tighter distribution than those that are (b) contiguously distributed.



11. Thermal data (ΔV_{DS}) versus void perimeter for fixed void areas of 10%, 30%, 50% and 70%.

over a single void of fixed area is greater for a circular shape than for a void of equal area but with an irregular boundary. This is one reason why heat dissipating active regions are laid out in a meandering finger pattern for power devices. Even with a uniform heat source, heat flow from the chip above a die bond void is affected such that temperature gradients develop from the center to the periphery of the void shape. The temperature data obtained with the IR microscope confirm this.

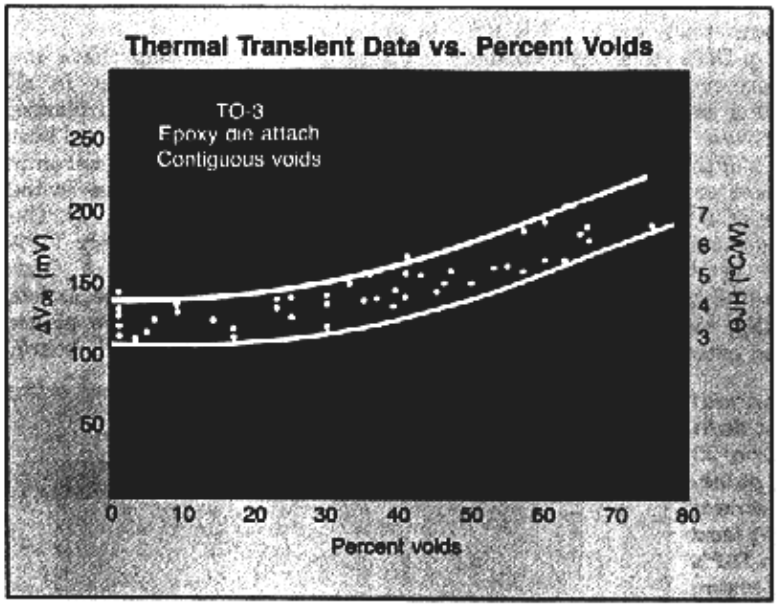
To further explain the variation between the contiguous and random bands of data in Figures 5 and 7, the void shapes were also considered, not just the void areas (i.e., percent voids) and sizes. The total void area and perimeter bounded by the voids were measured from the X-rays of the die bonds. Figure 10 presents scatter plots of void perimeter versus void area for the random and contiguous void cases. As expected, the smaller randomly voided samples tend to have larger void perimeters than contiguously voided samples with the same percent voids. Further, the random void band exhibits a tighter distribution. The relevance of void perimeter is evident when thermal resistance data are plotted versus void perimeter for various fixed void areas in Figure 11. The trend is similar for each band of data, namely increasing perimeter results in lower resistance. Further, the ratio of the void area to perimeter is able to represent all the data, both random and contiguous. The

scatter in the thermal data increases with percent voids, and is larger for the contiguous case than for the random case. This is because samples were assembled statistically, producing more widely varying void sizes and shapes as the percent voids increases.

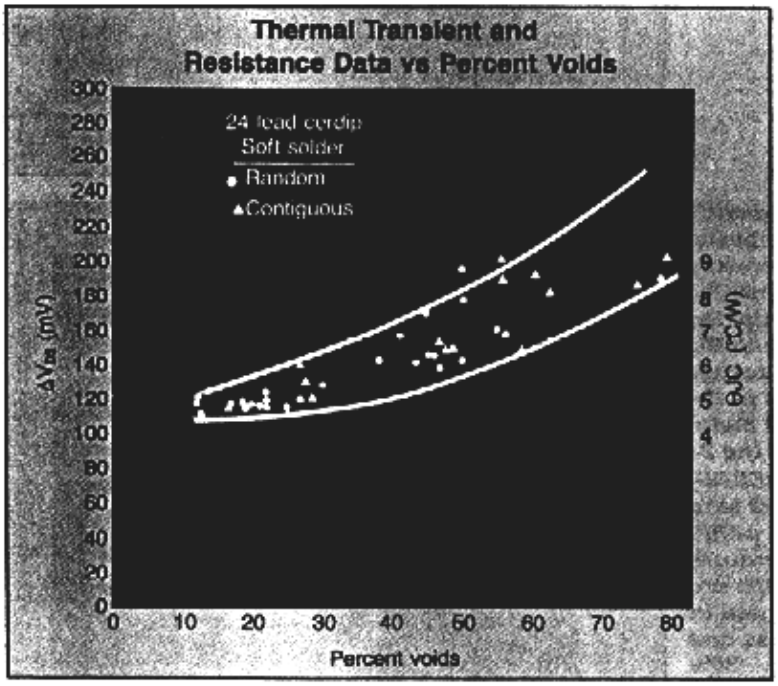
Aluminum TO-3/epoxy die attach

Measurements identical to those presented in Figures 5 and 7 for the Steel TO-3/soft solder case are summarized in Figure 12 for the Aluminum TO-3/epoxy die attach samples. The thermal transient measurements are plotted and a calibrated steady state thermal resistance scale is included on the right hand margin. The steady state scale was generated from measurement on selected samples similar to Figure 8. The increased thermal resistance compared to the Steel TO-3/soft solder case is due to both the lower thermal conductivity of the 5052 aluminum compared to OFHC copper and to the poor thermal characteristics of the conductive epoxy. In addition, the relatively large spread in ΔV_{DS} near 0% voids compared to the soft solder case suggests more sensitivity and/or less consistency in the process of epoxy bonding than in soft soldering. The spread in ΔV_{DS} remains relatively constant over the entire range of voids, in stark contrast to Figure 7. Also, the relative impact of these contiguous voids on thermal performance is quite small for less than 30% voids, becoming larger for void concentrations above 50%.

The narrow uniform band in Figure 12 suggests that the total percent voids is more important in determining the performance of these samples than the void perimeter arguments presented previously. This is partly because the void patterns were somewhat predetermined by painting the epoxy, as opposed to using a more random process such as solvent evaporation.



12. Thermal transient data (ΔV_{DS}) versus percent voids for TO-3 aluminum packages employing epoxy die attach and a 20 msec heat pulse.



13. Thermal transient and thermal resistance data for 24 pin CERDIP packages with soft solder die attach versus percent voids.

24 lead CERDIP

Both thermal transient and steady state thermal resistance (Θ_{JC}) data were obtained on a relatively small number of 24 lead CERDIP packages. Since the CERDIP package has poorer thermal performance than the TO-3 metal package, the relative effect of die bond voids is less on the package's total thermal resistance. The thermal data are plotted in Figure 13 as ΔV_{DS} versus percent voids and includes Θ_{JC} values obtained by the scanning IR method on the right hand margin. As with metal packages, both ΔV_{DS} and Θ_{JC} increase with percent voids, although the rate of increase is lower. For example, when voiding increases from 10% to 50%, Θ_{JC} increases by about 40% (5°C/W to 7°C/W), less than even the random TO-3 case. Another important difference in these data is the lack of separation between the random and contiguous cases. This is primarily due to difficulty in clearly separating random versus contiguous categories from the sample base.

40 lead p-DIP

The relative impact of die bond voids on a package's thermal resistance is strongly dependent on the package's overall thermal peformance. As already noted, the same degree of voiding

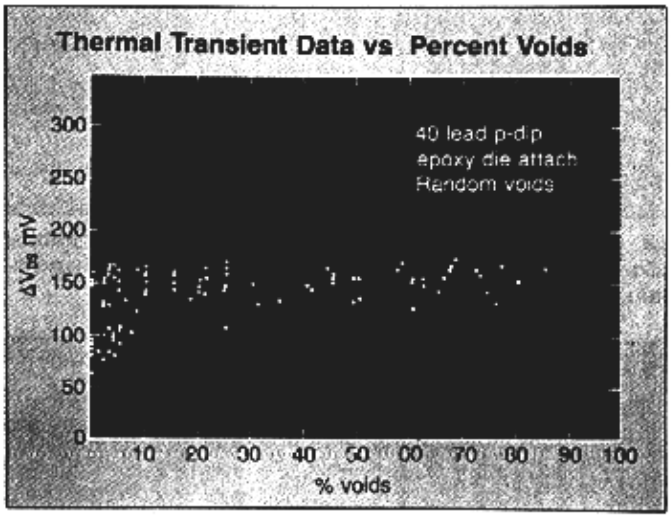
produced a greater effect in a metal TO-3 package than in a CERDIP package. In p-DIPs, this trend should continue where even less dependence of Θ_{JA} on voiding is expected. Detailed studies[4] proved that the thermal conductivities of the molding compound and lead frame controlled the thermal performance of a typical p-DIP, in a given external environment. A factor of 4.5 increase in thermal performance could be realized by judicious selection of the molding compound, lead frame material, and external air cooling in 16 lead p-DIPs, compared to a factor of 2.3 in 40 lead p-DIPs.

Plastic encapsulated chips have the advantage of dissipating heat in all directions into the overmolded plastic, as opposed to nearly unidirectional heat flow in most metal and ceramic packages. The disadvantage lies in the poor thermal conductivity of the overmold plastic, approximately 0.2% that of a copper header. A high conductivity copper lead frame assists heat spreading throughout the plastic and even carries heat to the PC board, but its cross-sectional area severely limits its effectiveness.

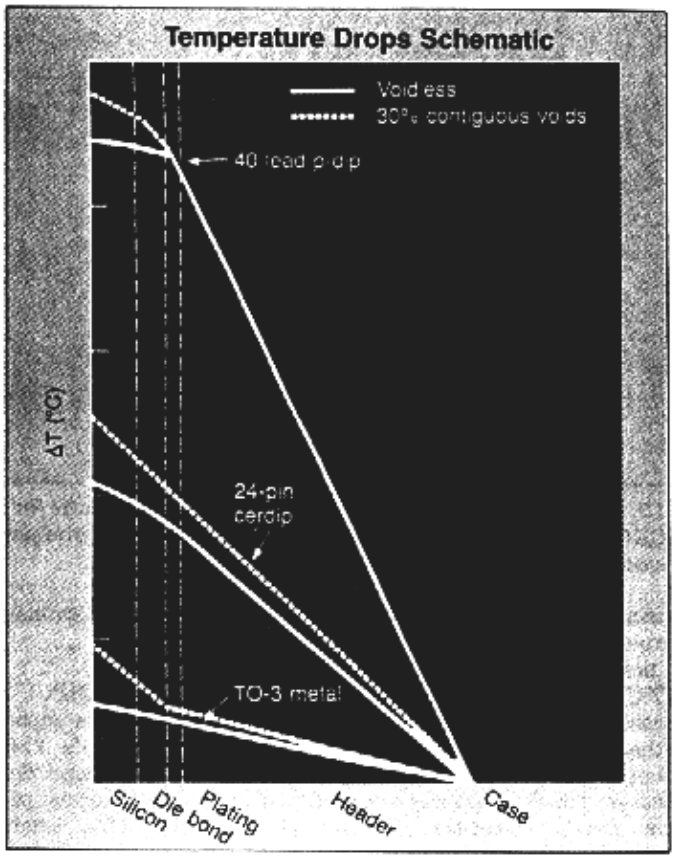
Figure 14 presents thermal resistance data versus percent voiding for a 40 lead p-DIP with a copper alloy lead frame, containing small, randomly dispersed voids. Except for excessive scatter observed at low void concentrations, these data suggest very little impact of small, random voids on package thermal resistance, even for void concentrations greater than 50%. In fact, the sample-to-sample scatter at a given percent voiding is much greater than the overall effect of void concentration. Following extensive cross sectioning, the large scatter at 0-10% voiding was found to be due to variations in the epoxy die attach thickness. Samples exhibiting larger ΔV_{DS} have die bonds over twice as thick as those with small ΔV_{DS}. Even much of the scatter for the higher percent voiding portion of the curve is attributable to die bond thickness radiations.

Data taken for contiguous voids in 40 lead p-DIPs exhibited a similar trend, to Figure 14, but with somewhat greater scatter and a slightly increasing ΔV_{DS} for void contents about 50%.

The thermal resistances were not higher than observed for the random voiding case, however, again underscoring the greater importance of die bond thickness in the p-DIPs as opposed to void concentration for acceptable thermal performance.



14. Thermal transient data (ΔV_{DS} for a 20 msec heat pulse) versus percent voids for 40 lead p-DIP's employing epoxy die attach.



15. Schematic showing temperature drops across the silicon chip, the die bond and the package materials in the TO-3 metal package, the 24 lead CERDIP and the 40 lead p-DIP. Temperature drops are illustrated in voidless and 30% (contiguous) voided packages.

Conclusion

Gross voiding in die bonds can significantly increase the peak junction temperature of a powered device, thereby impacting the long-term reliability. A strong interplay among the package construction, the die attach material, the overall void concentration and the specific void characteristics determine the actual effect of the voiding on device reliability. In general, packages in which the die bond plays the largest role in the overall thermal performance will be the most impacted by die bond voiding. Since metal packages house the highest powered devices and exhibit the lowest overall thermal resistance, they will be most sensitive to die bond voiding as illustrated in Figure 15. In the case of no voiding, the die bond already contributes significantly to the overall thermal resistance. When a relatively large contiguous void is present, the heat must flow around the void creating a large temperature gradient in the silicon and severely degrading the package's thermal performance. If the large void is instead broken up into

many smaller voids, the perturbation to heat flow is less with a much smaller temperature gradient induced in the silicon surface.

In poorer performing thermal packages such as the CERDIPs and even the p-DIPs, small concentrations of random voids have little effect on the peak junction temperature. Even larger concentrations of random voids should have little effect on most p-DIP packages. However, larger contiguous voids will degrade the thermal performance of all packages investigated, if large enough or in sufficient overall concentration. Therefore, voids are often tolerable thermally in the poorer performing packages, if they are small and distributed uniformly throughout the die bond. Large contiguous voids should be acceptable only when IR imaging techniques have proven that the peak junction temperature is below the acceptable limit. □

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