Monitoring Die-Attachment Integrity

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Traditional methods of evaluating the attachment integrity of die to substrate have been either destructive or vague. Thermal-transient testing is a non-destructive method that is fast and relatively simple, and can be used for 100% testing. Amenable to automation as well, it can be employed at a number of points in the manufacturing process, and also for users' incoming inspection.

The quest for quality in the manufacture of semiconductor devices and the products in which they are used has prompted renewed interest in the question of just how well semiconductor die are mounted on substrates or in packages. Both semiconductor manufacturers and users continue to seek new methods to monitor die-attachment integrity at lower cost and higher confidence levels. The traditional approaches — die shear and X-ray photography — leave much to be desired. To satisfy modern high-performance requirements, a new approach to the problem is needed.

Defining the Problem

Why is die-attachment integrity so important? The answer is simple — lower operating junction temperature! All other things being equal, the better the die attachment, the lower the junction temperature. Both theoretical and empirical results show that semiconductor-device long-term failure rates are directly related to junction temperature. For example, the failure probability for a semiconductor device operating at a temperature of 113°C will be twice as great as that for operation at only 100°C. Similar failure rate differences can be calculated for other operating temperatures.

Low-power integrated-circuit designs and technology — CMOS, for example — are usually regarded as being less susceptible to temperature failure mechanisms by virtue of their design. Often overlooked, however, are power densities and dynamic power requirements. Cramming more and more cells onto a given chip size, even assuming low-power cell design, increases the power dissipation per unit area, thereby raising junction temperature. Similarly, the trend toward higher cycle rates also increases power requirements and, hence, power dissipation.

Nor do linear integrated circuits escape junction-temperature-related problems. Offset current and voltage drift are junction-temperature dependent, and must be given adequate consideration to meet today's high-performance specifications. Monolithic power amplifiers and voltage regulators also suffer from junction-temperature problems, not only because they are power devices, but also because of increasing power densities as manufacturers shrink chip size in order to increase yields and reduce die cost.

Alternative Techniques

At the present time two basic techniques are used for monitoring die-attachment integrity. Each is well established and has a loyal following for many specific applications. The older of the two, die shear, is often referred to as "die push". By means of a small tool that often resembles a dentist's pick, sufficient force is applied to the edge of a mounted die either to push the die off its mounting or to fracture it. Subsequent inspection of the sheared or cracked die and the die mounting area can provide an approximate indication of how well the die was mounted. Long usage of the die-shear method and lack of a completely acceptable alternative have brought some sophistication to the method. Instruments are now available that can automatically apply an increasing shearing force up to a predetermined limit and/or indicate the force at which shear occurs.

Even with its present level of industry acceptance, the die-shear method presents several major problems. Because the method is basically destructive, it can be used on only a relatively small sample size from a given production run. Small sample sizes lead to low product-quality confidence levels. Moreover, difficulty is encountered in attempting to place the

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tool precisely on each die tested. Finally, interpretation of die-shear results is very subjective, and difficult to correlate with actual device performance.

The second, and newer, method of evaluating die-attachment integrity is X-ray photography. A mounted die/package (or substrate) combination is placed on a piece of photographic film and then subjected to a beam of X rays. Selection of the proper X-ray potential and focus depth produces a picture of the die attachment area on the film. Then either the film negative itself or a print made from it can be interpreted for void area as a percentage of total die mounting area. Figure 1 presents a number of such X-ray photographs of large bipolar transistor dice.

The X-ray method is burdened with many problems. Because it is difficult to distinguish exactly among the various light and dark areas, interpretation of the pictures is very subjective. Although basically not destructive, X-rays can damage certain types of semiconductor devices. For certain types of package or substrate materials, such as copper-based TO-3 packages that are very dense and X-ray absorbent, this method becomes practically useless. In addition, the X-ray photograph is only a two-dimensional view of a three-dimensional object — the attachment material. Its cost is often so great that the method is normally used on only a small sample basis in volume production applications. Only high reliability requirements and/or very expensive products can usually justify X-ray expense.

A summary of the problems associated with these two methods must include the fact that both are passive in nature. Neither actually investigates that function for which the die attachment to the mounting surface is primarily intended — heat flow. The vast majority of semiconductor devices in common usage rely on the back side of the semiconductor die for the removal of heat generated within the device junctions on the die. Without heat removal, junction temperatures would rise to destructive levels — or at least to a level that would significantly reduce operating life.

Thermal Transient Testing

During the past several years, thermal transient testing has come into vogue. In this method, a temperature-sensitive parameter (TSP) is measured both before and after the application of a heating power pulse. The difference between the initial and final TSP values is directly proportional to the junction-temperature change of the device under test (DUT). The TSP usually chosen is the forward-biased voltage of a junction within the DUT. Table I lists several of the more commonly used TSPs. The change in the TSP is commonly referred to as a differential voltage, ΔV.

Power is usually dissipated in the DUT by the application of voltage that would be used in normal circuit operation. The heating-power pulse width (duration) must be long enough to allow heat to propagate from the junction through the die to the die-attachment interface region, but short enough to avoid transfer of heat into the package. This provides the

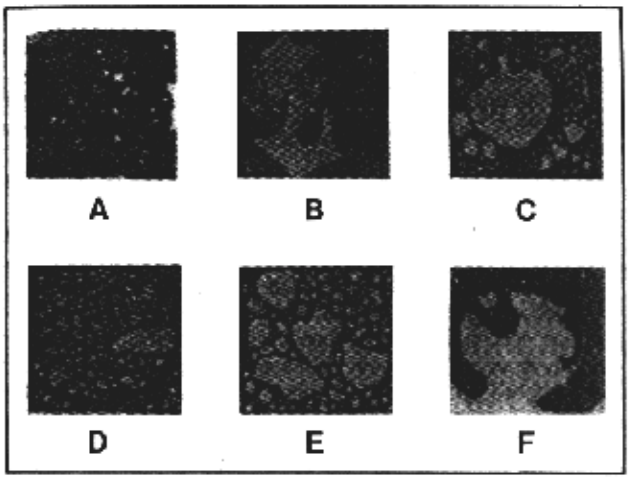

Figure 1. X-ray photographs of six large 0.250-in (6.35-mm) square bipolar transistor dice mounted on alumina substrates. Photographs are difficult to interpret with respect to percent void area—particularly for die with large void areas.

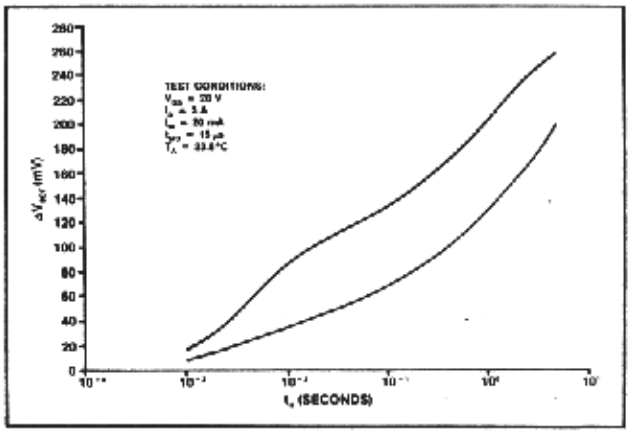

Figure 2. Typical heating curves for power MOSFETs. The two devices represented exhibit significantly different die-attachment integrity.

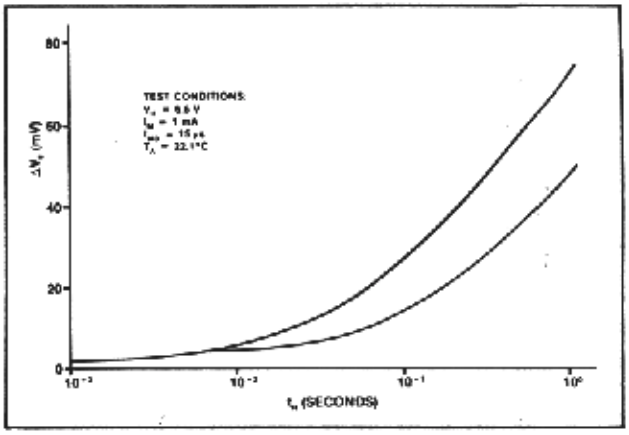

Figure 3. Heating curves for two bit-slice microprocessor devices that exhibit significant differences in thermal characteristics after heat flow has propagated through the device to the die-attachment region.

greatest sensitivity to die attachment variations. The heating-power pulse amplitude should be sufficient to cause a ΔV of at least 40 or 50 millivolts, corresponding to a 20°C or so change in junction temperature. Depending upon the device being tested, lower values of pulse amplitude may be necessary to avoid possible device damage.

Because this method actually monitors junction temperature changes due to applied power, there can be little doubt that it is measuring heat-flow characteristics. A well attached die will produce a lower ΔV value than a poorly attached die if the heating pulse width is chosen properly. Figures 2 and 3 show comparisons of typical "good" and "bad" die attachment cases for bipolar transistors and integrated circuits, respectively. Keep in mind that the thermal-transient test technique for die-attachment evaluation is applicable to *all* semiconductor devices — not just those shown in the examples.

Comparison of Methods

Table II compares the three die-attachment-evaluation methods described above. It is evident from this table that the thermal-transient method offers many

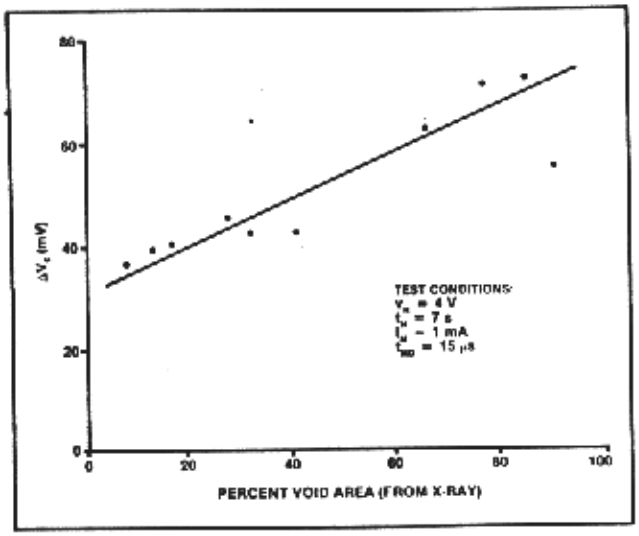

Figure 4. Comparison of thermal-transient (ΔV_F) and X-ray (percent-void-area) methods of evaluating die-attachment integrity, resulting from a detailed investigation. Tests were performed on a large number of gate-array chips, using the Sage Model D.A.E. 400 instrument. The chips measured approximately 0.2-in (5-mm) square, and contained approximately 5000 gates.

advantages. However, despite its clear-cut advantages, acceptance of the thermal-transient method has been rather slow at best. Slow acceptance can be traced to several causes:

- Lack of approved test-method standards. JEDEC and MIL-Std committees typically require considerable time to formalize a test method and receive industry approval. Suitable standards are in the final stages of completion and approval.
- Built-in inertia. The dynamic nature of the semiconductor industry does not always extend to portions of its assembly and test operations.

TABLE I—COMMON TEMPERATURE-SENSITIVE PARAMETERS

Device Type	TSP
Bipolar Transistor	V_{BE}
Junction FET	V_{GSF}
MOSFET	V_{BCF}
PN Diode	V_F
Schottky Diode	V_F
LED & Laser Diode	V_F
PIN Diode	V_F
Varactor Diode	V_F
Gunn Diode	V_{LF}
IMPATT Diode	V_{BR}
Thyristor (SCR, Triac, etc.)	V_{AK}
Integrated Circuit	V_F (substrate diode)

TABLE II—COMPARISON OF 3 MONITORING METHODS

	Die-Shear	X-Ray	Thermal-Transient
Destructive?	Yes	Maybe	No
Test Time	Few minutes	Several minutes (includes film development)	< 1 second
Data Interpretation Type	Subjective	Subjective	Objective
Data Interpretation Speed	Fast	Slow	Very Fast
Measurement Type	Static	Static	Dynamic
Applicable Point in Manufacturing	Following die attachment	Any time before complete encapsulation in most cases	Any time
Suitability	All devices	Not all chip/package combinations	Almost all devices
Sample Size	Very small	Can be 100% (typically much smaller)	100%
Amenable to Automated Testing?	No	No	Yes

TABLE III—X-RAY/ΔV COMPARISON

X-Ray Photo (Fig. 1)	V_{BE} (millivolts)
A	69
B	176
C	203
D	75
E	125
F	170

Test Conditions:
t_H = 20 ms;
V_H = 15 V;
I_C = 2.5 A;
I_M = 10 mA;
t_{MD} = 15 μs.

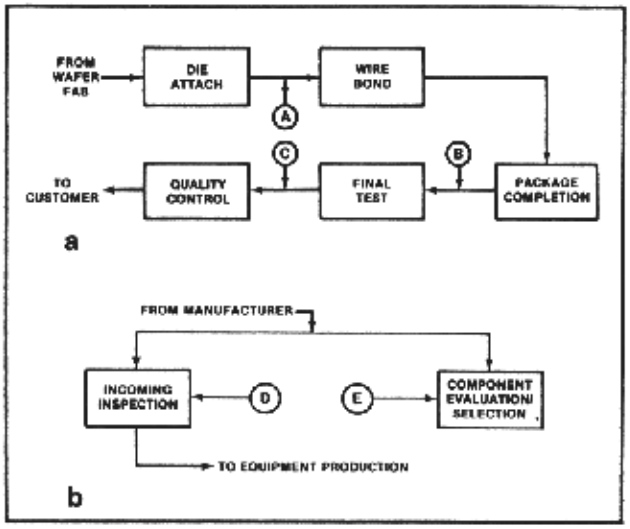

Figure 5. Block diagrams of the manufacturing process from just-attached die to final device use. The most logical die-attachment-evaluation monitoring points are shown circled for the semiconductor manufacturer (a) and the semiconductor device user (b).

- Lack of knowledge and awareness. Many people in the electronics field have inadequate knowledge of the thermal considerations involved in the proper design and application of semiconductor devices. This, in turn, reduces their sensitivity to and awareness of the potential that exists for device problems that are thermally related.

Current events that are occurring in the semiconductor/electronics industry will probably provide the impetus for an accelerated rate of thermal-transient-test acceptance. Competitive pressures on both quality and price are forcing semiconductor manufacturers to pay more attention to assembly procedures that are needed to build better devices at lower cost. In a similar vein, semiconductor users are performing more incoming-inspection testing on components to ensure conformance with electrical and quality requirements before these components are built into or installed in their equipment. Competitive pressures are also increasing the demand for knowledge about thermal characteristics of semiconductor devices, and are making both manufacturers and users more aware of thermal problems.

Figure 4 shows a correlation of results between X-ray and thermal-transient methods of evaluating die-attachment integrity. Similar correlation can be achieved between thermal-transient and die-shear methods. Table III indicates how difficult it can be to interpret X-ray photographs — particularly in the case of distributed die-attachment voids.

TABLE IV—DIE-ATTACHMENT MONITORING POINTS

Test Point (Fig. 5)	Test Type	Comment
A	Sample or 100% by manual or semi-automatic probing	Best place to test for die-attachment integrity because part has least value added
B	Sample or 100% by manual test station or semi-automatic device handler	Good point to test parts requiring very long final test times
C		Good point to test parts requiring short final test times
D		Can incorporate thermal-transient test into parametric/functional testing; screens out potential thermal problems before device goes into equipment
E	Probably 100% on small sample to characterize/ compare parts	Can test parts under power conditions at or near actual intended circuit operation

Application of Thermal-Transient Testing

Because a thermal-transient test employs an electronic instrument that requires only electrical connection to (rather than physical contact with) the device under test, the test can be performed at any one of several points in a manufacturing process, as shown in Fig. 5 and explained in Table IV. Immediately following die attachment (point A) is probably the best point at which to perform the test, for several reasons. This is the point of least value added to the device — before wire bonding, package completion, and final test. Here thermal-transient testing can be implemented on a 100% basis using automatic probing equipment, or on a sample basis with a manual probe station. Although the former is potentially the most desirable, it requires considerable capital equipment and development for proper implementation. The latter approach is relatively easy to install and put into operation. Being non-destructive, quick, and very objective (once acceptable ΔV limits have been established), thermal-transient testing facilitates the use of much greater sample sizes at low cost, resulting in higher product-quality confidence levels. Testing at this point in the assembly process also offers the possibility of die-attachment repair or package salvage.

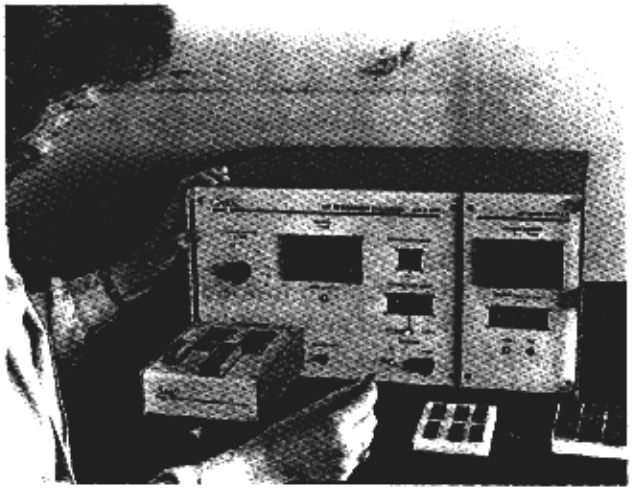

Figure 6. Typical die-attachment-evaluation test station for testing integrated circuits employs the Sage Model D.A.E. 400/012/017 instrument together with the T.F. 40 universal DIP test fixture. Using manual device insertion and removal, typical device test time is less than 2 seconds.

Testing for die-attachment integrity just before or at final test is most easily implemented. A very simple setup for evaluating completely packaged integrated circuits is shown in Fig. 6. A suitable instrument, such as the one illustrated in Fig. 6, can be interfaced easily to an automatic device handler for stand-alone operation, or it can be multiplexed with an automatic electrical tester in final-test applications. Semiconductor users can employ either approach as part of their incoming-inspection testing.

The last vestige of a "black art" in the semiconductor industry — the die attachment process — is now drawing increasing attention as quality and cost considerations gain greater prominence. Thermal-transient testing alone won't solve all of the problems, but it will provide a more scientific approach to monitoring die-attachment integrity.

Bernard S. Siegal *received the BEE degree from Cornell University, the MSEE degree from San Jose State University, and the MBA degree from the University of Santa Clara. He has held technical positions with Varian Associates, Hewlett-Packard, Microwave Associates, Siliconix, Intersil, and others. Mr. Siegal has published more than 40 technical articles in the areas of semiconductor device circuit applications, device operation, and testing techniques. He has also presented technical seminars on the thermal aspects of semiconductor devices. Mr. Siegal founded Sage Enterprises, Inc., Mountain View, CA in 1975.*